RL-TR-93-25
Final Technical Report
April 1993

VLSI DESIGN FOR RELIABILITY-HOT CARRIER EFFECTS

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	April 1993	Final Jun 91 - Jun 92

4. TITLE AND SUBTITLE
VLSI DESIGN FOR RELIABILITY-HOT CARRIER EFFECTS

5. FUNDING NUMBERS
C - F30602-91-C-0053
PE - 62702F
PR - 2338
TA - 01
WU - P9

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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory (ERDD)
525 Brooks Road
Griffiss AFB NY 13441-4505

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
RL-TR-93-25

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Martin J. Walter/ERDD/(315)330-4102.

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

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In order to simulate the reliability of MOS circuits, both the detailed model and the macromodel are used; the detailed model is used for accurate analysis of small circuits and the macromodel is used for very large circuits for computational efficiency. Since the hot-carrier-induced aging of MOS circuits is input-pattern dependent, an important task is to develop a computationally efficient probabilistic timing approach to hot-carrier-effect estimation without resorting to the Monte Carlo simulation. We have developed a new probabilistic approach that accounts for cumulative effects of all input waveform combinationsin a single run.

In an effort to simulate ultra-large-scale circuits with over one-million transistors,
(continued on reverse)

14. SUBJECT TERMS	15. NUMBER OF PAGES
VLSI reliability, hot-carrier effects, computer aided design	80
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. Z39-18
298-102

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Final Report Evaluation

VLSI Design For Reliability - Hot Carriers Effects
Contract F30602-91-C-0053

The growth in the use of custom, semi-custom, and application specific ICs (ASICs) in AF systems has brought several changes to the reliability qualification process. This occurred because the costs associated with reliability characterization have become a major part of the device cost when there are only a few hundred or thousand of such devices produced. Further, the cost of a second or third pass at fabrication, electrical-test and reliability qualification is very time consuming as well as expensive.

Analyzing an IC design for susceptibility to life limiting failure mechanisms is one approach to enhance the probability that at the end of the first pass of the design/fabricate/test/evaluate reliability cycle, the device will have an acceptable reliability.

This effort describes the modeling of the hot-carrier induced degradations of n-channel MOSFETS and the applications of those models to a variety of test circuits(CMOS). The degradation has been modeled at the device level, at the macromodel level and by applying statistical simulation methods. Circuit design parameters have been identified which affect the degradation.

Other efforts sponsored by Rome Lab in the area of design for reliability include statistical simulation techniques for current density estimation in conductors for electromigration analysis and worst case voltage drop and also an effort to develop rules based on design parameters such as fan-out and input slew rate to identify poor or likely areas of hot carrier degradation.

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VLSI DESIGN FOR

RELIABILITY-HOT CARRIER EFFECTS

Final Report

Account No. 93928-30/Order No. RI-68909X

Contract F30602-91-C-0053 (Task N-1-5702)

Abstract

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In an effort to simulate ultra-large-scale circuits with over one-million transistors, we have also developed new macromodels for hot-carrier-damaged logic gates such as inverters and transmission gates. In these macromodels, the level of hot-carrier damage is expressed in terms of the transistor size (W), output loading capacitance (C_L), and the input slew rate (a). Thus, for a given circuit, the level of hot-carrier-induced long-term degradation can be predicted by monitoring the input slew rate (a) and the ratio of W/C_L. This method can be applied to worst-case analysis of hot-carrier effects in ultra-large scale MOS circuits. Currently, a fast reliability rule checker is being developed for MOS circuits with more than one-million transistors.

I. INTRODUCTION

As the complexity and the density of VLSI chips increase with shrinking design rules, the evaluation of long-term reliability of MOS VLSI circuits is becoming an important problem. The assessment and improvement of reliability on the circuit level should be based on both the failure mode analysis and the basic understanding of the physical failure mechanisms. While some of the degradation mechanisms, such as electromigration and electrostatic discharge, manifest themselves by abrupt and catastrophic changes in the device characteristics and the circuit operation, other mechanisms, such as hot-carrier effects, cause noncatastrophic failures which develop gradually over time and change the circuit performance [1]-[3].

It is being recognized that important reliability issues other than the post-manufacture reliability qualification have to be addressed rigorously in the design phase. The development and use of accurate reliability simulation tools are therefore crucial for early assessment and improvement of circuit reliability: Once the long-term reliability of the circuit is estimated through simulation, the results can be compared with predetermined reliability specifications or limits. If the predicted reliability does not satisfy the requirements, appropriate design modifications may be carried out to improve the resistance of the devices to degradation. This cycle may be repeated several times until the simulated reliability of the circuit meets the desired specifications. The ultimate goal of CAD for reliability is to develop user-friendly and useful software tools that can be readily integrated into existing CAD frameworks and environments.

The hot-carrier-induced degradation of MOS transistor characteristics is one of the primary mechanisms affecting the long-term reliability of MOS VLSI circuits. It is likely to become even more critical in the future-generation chips, since the scaling of transistor

dimensions without a proportional scaling of the power supply voltage (so-called constant-voltage scaling) aggravates this problem [4],[6]. The extent of the hot-carrier damage that each transistor experiences is determined by its terminal voltage waveforms, i.e., by the operating conditions of the circuit. The gradual degradation of device characteristics ultimately leads to the degradation of circuit performance over time. Consequently, the mechanism of hot-carrier-induced device degradation must be examined within the context of circuit simulation.

The reliability simulation should determine how the overall circuit performance is affected as a result of device aging, and which devices are most likely to cause critical circuit performance failures. The framework for a hot-carrier reliability simulation tool involves (i) modeling the gate oxide degradation in the MOS transistor as a function of its operating conditions, (ii) modeling the behavior of the MOS transistor with localized oxide damage, (iii) simulation of gate oxide degradation during long-term circuit operation, and (iv) determination of the overall circuit performance after hot-carrier stress. The integration of these components into a simulation framework is a prerequisite for accurate prediction of the long-term circuit reliability characteristics.

Early attempts at modeling the hot-carrier-induced device degradation mechanisms were concentrated on modeling the MOSFET gate current I_G, since this current was assumed to be a good indicator of the injected hot-carrier density [2]. However, experimental results have failed to demonstrate any significant correlation between the gate current and the device degradation. On the other hand, a close correlation between the substrate current and the degradation level was found under various stress conditions [3]. Based on the rate equations governing the generation of interface states, Hu *et al.* [6] have proposed a semiempirical

relationship between the interface trap density and the substrate current of the transistor under static operating conditions. This relationship has been widely used for estimating the *lifetime* of the transistor, defined as the time required for the *threshold voltage* of the transistor to reach a predetermined limit value [3],[6],[11]. Later, the same approach has been used for the determination of device lifetime under dynamic operating conditions by Hu *et al.* [12] and by Weber [13].

Several attempts have been made to apply the device lifetime estimation methods mentioned above to circuit reliability simulation. Hohol and Glasser have estimated the amount of hot-carrier-induced degradation by monitoring the gate current of the MOS transistors [14]. Later, Kuo *et al.* [15] have proposed a quasi-static device lifetime estimation approach, which is based on the semiempirical interface trap generation equations. The hot-carrier reliability simulator HOTRON developed by Aur *et al.* also follows a similar approach [11]. The quasi-static lifetime estimation scheme is based on the fundamental assumption that the operating conditions (i.e., terminal voltage waveforms) of each transistor remain unchanged during the entire operation interval. As a result, its realistic application to circuit reliability simulation is fairly limited. A further drawback of this approach is that it focuses on the estimation of individual transistor lifetimes rather than on the estimation of circuit performance degradation over time. A different simulation method has been proposed by Sheu *et al.* [24] to overcome the deficiencies of the quasi-static lifetime estimation approach by repeating the long-term simulation at several projected time points, while updating the affected device parameters at each step. However, this method requires periodic updating of more than 15 different BSIM model parameters; thus, the simulation of circuit performance after hot-carrier damage relies on extensive parameter extraction under different stress conditions prior to

simulation. The hot-carrier reliability simulator designed for this task consists, in addition to the circuit simulator, of various pre- and post-processor modules to facilitate the periodic updating of device model parameters [25].

In this report, an integrated simulation approach is presented for estimating the hot-carrier-induced degradation of MOSFET device characteristics and circuit performance. The transistor degradation model used in simulation incorporates a one-dimensional MOSFET model for representing the electrical behavior of locally damaged transistors. The hot-carrier-induced oxide damage can be specified by only a few parameters, avoiding extensive parameter extractions for the characterization of device damage. The physical degradation model used in the proposed simulation tool includes both of the fundamental degradation mechanisms, i.e., charge trapping and interface trap generation. A repetitive simulation scheme has been adopted to ensure accurate prediction of the circuit-level degradation process under dynamic operating conditions. The evolution of hot-carrier-related damage in each device is automatically simulated at predetermined time intervals, instead of extrapolating the long-term degradation using only the initial simulation results.

The hot-carrier reliability simulation tool provides information on

(i) the evolution of device and circuit performance degradation during dynamic operation,

(ii) the amount of hot-carrier-induced damage in each transistor after a specified operation period, and

(iii) the performance characteristics of the damaged circuit.

This information can be used both for understanding the circuit-level dynamics of the degradation mechanisms and, as a design aid, for improving the long-term reliability through design

modifications. The simulation results can also be applied to the reliability characterization of various circuits and to the development of simple macromodels to represent their long-term behavior.

The hot-carrier injection mechanisms leading to oxide damage in MOSFET devices, physical models for quasi-elastic scattering and impact-ionization mechanisms and an oxide interface degradation model will be briefly reviewed for self-sufficiency.

A. Hot-Carrier Injection Mechanisms and Models

Our work is focussed on nMOS transistors, for which the hot-carrier effects have been observed to be more significant than for pMOS transistors [6],[7].

The hot-carrier-related degradation of the I-V characteristics of MOS transistors is attributed to two fundamental mechanisms: (i) charging of oxide traps (charge trapping), and (ii) generation of new oxide-interface traps [8],[9]. Two mechanisms have been identified as being responsible for the injection of charged particles (electrons and holes) into the gate oxide. These mechanisms are (i) quasi-elastic scattering of channel hot electrons, and (ii) creation of high-energy electron-hole pairs by impact ionization.

A.1. Quasi-elastic scattering of hot electrons

The following physical model for hot-electron injection in nMOS transistors is based on the lucky-electron concept [10]. A certain percentage of the electrons moving along the channel from the source to the drain may enter the gate oxide. For channel hot electrons to reach the gate oxide, they must gain sufficient kinetic energy from the channel electric field and have their momentum redirected towards the $Si–SiO_2$ interface to surmount the potential bar-

rier. To quantify the probability that these electrons could be injected into the gate oxide, several types of scattering events are considered.

The first event to be considered is the acceleration of a channel electron by the lateral electric field along the channel. When the hot electron reaches the drain end of the channel, its momentum has to be redirected toward the interface by a collision. It must be noted that this redirecting collision should not be an energy-robbing collision, so that the electron will retain the kinetic energy required to surmount the $Si–SiO_2$ potential barrier. The term *quasi-elastic scattering* has been used in that context. Following the redirecting collision, the electron must travel from the point of collision to the oxide interface without suffering further collisions which would redirect its momentum or diminish its kinetic energy. If the electron reaching the oxide interface has a sufficient kinetic energy to overcome the oxide potential barrier, it is injected into the gate oxide. Since these events are assumed to be statistically independent, the injection probability can be obtained as the product of the probabilities of each event.

A simplified one-dimensional model of this mechanism has already been used for modeling the gate electron current in nMOS transistors by Tam *et al.* [18]. However, the gate current consists only of electrons that overcome the image potential well in the oxide and reach the gate electrode. In fact, a large percentage of the electrons entering the gate oxide are either scattered in the oxide and/or are returned to the silicon substrate by the opposing electric field [19].

High-energy electrons injected into regions of opposing oxide electric field can still contribute to charge trapping and interface trap generation in the oxide, although the large majority of these electrons are repelled back into the substrate by the oxide electric field. The

importance of electron injection under opposing oxide electric field conditions has been first noted by Hofmann *et al.* [19]. In the following, a one-dimensional model will be introduced for the electron injection based on quasi-elastic scattering of electrons. For reasons explained above, the electron injection current I_{ei} is believed to be a better indicator of the hot-carrier damage than the gate current.

Based on the scattering probability components explained earlier, a simple injection current expression is proposed as follows.

$$I_{ei} = \frac{1}{2} I_{DS} \frac{t_{ox}}{\lambda_r} \left[\frac{\lambda E_m}{\Phi_b}\right]^2 P_{inj}(E_{ox}) \exp\left[-\frac{\Phi_b}{E_m \lambda}\right]. \quad (1)$$

Here, E_m denotes the maximum channel electric field in the direction of the channel current I_{DS}, and Φ_b denotes the $Si–SiO_2$ potential barrier height. These quantities are defined as

$$E_m = \frac{V_{DS} - V_{DSAT}}{\sqrt{3 \cdot t_{ox} x_j}} , \quad (2)$$

$$\Phi_t = 3.2 - \beta \sqrt{E_{ox}} - \theta E_{ox}^{2/3} , \quad (3)$$

where

$$E_{ox} = \frac{V_{GS} - V_{DS}}{t_{ox}} . \quad (4)$$

Other physical parameters used in Eqs. (1)-(4) are: the scattering mean-free path of the hot-electron $\lambda = 9.2$ nm, the redirection mean-free path $\lambda_r = 61.6$ nm, the barrier lowering coefficient $\beta = 2.59 \times 10^{-4}$ $(V\ cm)^{1/2}$, and the tunneling probability between silicon and silicon dioxide $\theta = 4 \times 10^{-5}$ [18].

The most important term in Eq. (1) is $P_{inj}(E_{ox})$, which denotes the probability that a hot electron can enter the gate oxide by overcoming the potential barrier. The probability of oxide scattering is neglected because this process does not affect the number of hot electrons *entering* the gate oxide [20]. High-energy electrons can be injected into the oxide despite the repelling oxide electric field. An empirical expression for the probability $P_{inj}(E_{ox})$ is given as [18]

$$P_{inj} \approx \frac{\alpha E_{ox}}{\left[1 + \frac{E_{ox}}{\beta}\right]} \times \frac{1}{\left[1 + \frac{\gamma}{L_{eff}} e^{-E_{ox} t_{ox}/1.5}\right]} + \eta \tag{5}$$

for $E_{ox} \geq 0$ and

$$P_{ox} \approx \eta \tag{6}$$

for $E_{ox} < 0$,

where $\alpha = 5.7 \times 10^{-6}$, $\beta = 1.5 \times 10^{5}$, $\gamma = 2 \times 10^{-3}$ and $\eta = 2.5 \times 10^{-2}$. If the oxide scattering probability is also considered in the derivation of the combined injection probability, the resulting expression yields P_{gate} for an electron to overcome the oxide-interface potential barrier *and* to reach the gate electrode. Thus, Eq. (5) can also be used for modeling the gate current in an nMOS transistor, by substituting the probability coefficient P_{inj} with P_{gate}.

A.2. Impact ionization by hot electrons

When the nMOS transistor is operating in the saturation region, a certain percentage of the hot electrons moving horizontally along the channel create electron-hole pairs by impact ionization near the drain. The holes created by this process (also called avalanche pair

production) are collected by the substrate, creating the drift component of the substrate current. While most of the created electrons are attracted toward the drain junction, some high-energy electrons and holes are injected into the gate oxide, and contribute to oxide degradation. The substrate current can provide only a rough indication for the amount of the oxide damage that is caused primarily by the electrons generated by impact ionization and injected into the gate-oxide interface. In particular, the injected hot carriers must have kinetic energies exceeding a critical energy to form fast interface traps upon injection.

The amount of impact ionization at the drain end of the channel under given operating conditions can be evaluated by using the lucky-electron concept as in the previous section. Let $\Phi_{it,e}$ and $\Phi_{it,h}$ be the critical energies for electrons and holes, respectively, to form fast interface traps upon injection. Experimentally determined values for these critical energies are $\Phi_{it,e} = 3.7$ eV and $\Phi_{it,h} = 4.2$ eV [16]. Approximating the high-energy tail of the electron energy distribution by Maxwell-Boltzmann statistics, the current density which consists of electrons with kinetic energies higher than $\Phi_{it,e}$ can be expressed as the bond-breaking electron current density $I_{BB,e}$.

$$I_{BB,e} = \frac{C_1}{W} I_{DS} \exp\left[- \frac{\Phi_{it,e}}{q\lambda_e E_m} \right]. \tag{7}$$

Here, E_m represents the maximum lateral electric field along the channel, which is defined by Eq. (2), and λ_e represents the mean-free path for electrons. Similarly, the portion of the hot-hole current density, which consists of holes with kinetic energies higher than $\Phi_{it,h}$, can be approximated by

$$I_{BB,h} = \frac{C_2}{W} I_{SUB} \exp\left[- \frac{\Phi_{it,h}}{q\lambda_h E_m} \right] \quad (8)$$

where λ_h represents the mean-free path for holes [16].

The relationship between the bond-breaking current and the substrate current I_{SUB} has been studied extensively. The value of the coefficient C_1 can be found easily by comparing Eq. (7) with measured substrate currents. If I_{SUB}/I_{DS} is plotted against $1/(V_{DS} - V_{DSAT})$ on a semilogarithmic plot, the y-axis intercept of the best linear fit to this curve gives the value of C_1. Experimental results indicate that C_1 is between 1.9 and 2 [6],[16]. The values of the electron and hole mean-free paths are $\lambda_e = 6.7$ nm and $\lambda_h = 4.9$ nm.

B. Oxide-Interface Degradation Mechanisms and Models

Recent studies have shown that two distinct voltage regions of stress can be identified for nMOS transistors, indicating different types of degradation mechanisms. For the region of maximum substrate current ($V_{DS} \approx 2 \cdot V_{GS}$), the oxide damage has been linked to the interface trap generation through hot electrons and hot holes, and no significant charge trapping could be observed [6],[8],[9],[16]. For the region of maximum electron injection into oxide ($V_{DS} \approx V_{GS}$), the damage is caused to a great extent by charge trapping, and also by moderate interface trap generation [8],[9]. Consequently, an investigation of hot-carrier-induced degradation mechanisms must encompass the charge trapping and the interface trap generation in nMOS transistors, both of which are caused by hot carriers injected into the gate oxide.

Experimental data obtained with gate and drain voltage amplitudes of ≥ 5 V indicate that the degradation rate of nMOS transistors during dynamic (AC) operation is larger than the degradation rate during static (DC) operation. This enhanced degradation has been attributed

to alternating hot-electron *and* hot-hole injections into the gate oxide under dynamic stress [8],[9],[13]. However, the probability of hot-hole injection is significantly reduced if the power supply voltage is limited to $V_{DD} \leq 5$ V, as in most CMOS VLSI circuits, because the potential barrier height for holes at the interface is approximately 4.6 eV. Thus, the enhancement of device degradation for dynamic stress conditions is considered in the following models.

B.1. Charge trapping into oxide traps

The charge distribution and the charge density in the gate oxide are altered when excess electrons or holes are captured by the existing traps in the oxide. The oxide-charge distribution can also be changed by the impact release of a trapped electron or hole by a hot carrier. Hot-carrier stress experiments conducted by Sah *et al.* on MOS capacitors with various types of oxides have indicated a close relationship between the trapped oxide-charge density N_{ox} and the injected electron fluence N_{inj}, which is defined as the integral of the electron injection current density over time [1],[5], i.e.,

$$N_{inj} = \int_0^t J_{ei}(\tau)\, d\tau. \tag{9}$$

Here, J_{ei} denotes the electron injection current density. The oxide-charge trapping, as a function of the avalanche injected electron fluence, can be expressed by a least squares fit to the general multitrap first-order kinetic equation,

$$N_{ox}(N_{inj}) = \sum_i N_i \left[1 - \exp\left(-\sigma_i N_{inj}\right) \right]. \tag{10}$$

In this expression, N_{ox} is the trapped oxide-charge density, N_i is the areal trap density and σ_i is the effective capture cross-section area. This multitrap model is adequate for charge trapping without anomalous positive turn-around charge. Even a single-term expression usually provides a satisfactory fit to the measured characteristics. For simple simulation purposes, a two-term kinetic equation has been used to express the relationship between the trapped charge density and the injected electron fluence [20]. For the two-term (i = 2) kinetic equation, the areal trap density and effective capture cross-section coefficients are given as $N_1 = 1.58\times10^{12}$ cm^{-2}, $N_2 = 1.36\times10^{12}$ cm^{-2}, $\sigma_1 = 450\times10^{-20}$ cm^2 and $\sigma_2 = 100\times10^{-20}$ cm^2.

The charge trapping mechanism described above was regarded to be of lesser significance previously and was neglected in most of the hot-carrier reliability simulation approaches. However, recent experimental evidence indicates that charge trapping must be considered as a significant degradation process, especially under dynamic stress conditions where both charge trapping and interface trap generation were found to be contributing simultaneously to device degradation [9].

B.2. Interface trap generation

Interface traps (states) are generated in nMOS transistors by hot electrons as well as by hot holes, which upon injection into the Si–SiO_2 interface break the electron-pair bonds. The resulting interface trap, also called fast interface state, may easily acquire an electron when the device is in strong inversion, and become negatively charged. Thus, the charge distribution in the oxide interface is largely influenced by the existence of the interface traps.

The field of possible trap generation mechanisms can be narrowed by assuming that the breaking of silicon-hydrogen bonds by hot electrons is the dominant mechanism of trap

generation [6]. This mechanism is symbolically depicted in Fig. 1. The rate of bond breakage by hot electrons may be expressed as ($K \cdot I_{BB,e}$). The coefficient K is proportional to the density of the silicon-hydrogen bonds at the interface. The rate of Si^* and H recombination may be expressed as ($B_p N_{it} n_H(0)$), where N_{it} is the interface trap density, $n_H(0)$ is the concentration of H at the interface and B_p is a process-dependent constant. Thus, the net rate of interface trap generation is

$$\frac{dN_{it}}{dt} = K\, I_{BB,e} - B_p\, N_{it}\, n_H(0). \tag{11}$$

Also, the rate of interface trap generation is equal to the rate of interstitial hydrogen diffusing away from the interface, which can be approximated with

$$\frac{dN_{it}}{dt} = D_H\, n_H(0)/X_H. \tag{12}$$

Here D_H and X_H are the effective diffusion constant and the effective diffusion length of hydrogen, respectively. Combining Eqs. (11) and (12), the following differential equation is obtained:

$$\frac{dN_{it}}{dt}\left[1 + B_p \frac{X_H}{D_H} N_{it}\right] = K\, I_{BB,e}. \tag{13}$$

This equation describes the long-term interface trap generation process by hot-electron injection, under static operating conditions.

Note that the coefficient K determines the rate of bond breakage by electrons. It is assumed that the generated interface traps are acceptor-type, i.e., they become negatively

charged by capturing an electron during strong inversion of the channel. The coefficient values used in the simulations are $B_p X_H/D_H = 10^{-8}$ cm^2, and $K = 5\times10^{15}$ [21].

B.3. Trap generation under dynamic operating conditions

The process of interface trap generation has usually been modeled for static or quasi-static stressing conditions. Assuming that the electron bond-breaking current does not vary significantly over time, Hu *et al.* have approximated the solution of Eq. (13) by the following simple power-law expression [6]

$$N_{it}(t) = C \left[I_{BB,e}\, t \right]^n. \tag{14}$$

Here, C represents a process-dependent constant, and the exponent n is in the range of 0.5-1. Expressing the bond-breaking current in terms of the substrate current, Eq. (14) can be rewritten as

$$N_{it}(t) = C' \left[\left(\frac{I_{SUB}}{I_{DS}} \right)^{\frac{\Phi_it}{\Phi_i}} I_{DS}\, t \right]^n. \tag{15}$$

This expression has been widely used for estimating the hot-carrier-induced interface trap generation in nMOS transistors under various operating conditions and for relating the amount of hot-carrier damage to the substrate current and to the stress time t. Equation (14) has also been used for quasi-static simulation of MOSFET degradation under dynamic operating conditions by replacing the bond-breaking current density $I_{BB,e}$ with its time-averaged value $\langle I_{BB,e} \rangle$ over one cycle [11],[13],[15]. However, the use of this single semiempirical expression to account for several different degradation processes can not be justified for the general case.

In a circuit environment in which the transistors are experiencing dynamic hot-carrier stress, the operating conditions of all devices are expected to shift in time as the device characteristics deteriorate. This fact has been neglected in most of the hot-carrier stress simulation approaches. The proposed trap generation model has to be modified to allow the estimation of interface trap generation under dynamic operating conditions, where the bond-breaking current waveforms are, in general, rapidly changing over time.

In the following, the terminal voltage waveforms of the MOSFET are assumed to be periodic, with a period length of T_0. At first, we consider the amount of interface trap generation within one cycle (period) of length $T_0 = t_{n+1} - t_n$, in which the dependence of $I_{BB}(t)$ on N_{it} is negligible. Both sides of Eq. (13) can be integrated over the time period T_0, which results in the following expression:

$$\int_{N_{it}(t_n)}^{N_{it}(t_{n+1})} \left[1 + B_p \frac{X_H}{D_H} N_{it} \right] dN_{it} = K \int_{t_n}^{t_{n+1}} I_{BB}(t)\, dt. \tag{16}$$

Further manipulation of Eq. (16) leads to a simple differential equation describing the long-term dynamics of interface trap generation [21]

$$\frac{dN_{it}}{d\tau} \left[1 + B_p \frac{X_H}{D_H} N_{it} \right] = K \langle I_{BB} \rangle, \tag{17}$$

where $\langle I_{BB} \rangle$ is the average value of $I_{BB}(t)$ over one period. As the stress conditions of the device change during long-term dynamic operation, the deviations in the trap generation rate can be accounted for by modifying the right-hand side of Eq. (17).

II. SIMULATION OF DEVICE AND CIRCUIT PERFORMANCE DEGRADATION DUE TO HOT-CARRIER EFFECTS

A most significant difficulty pertaining to the circuit-level simulation of hot-carrier effects lies in the very slow rate at which device degradation progresses. The time period required for the development of a measurable amount of degradation in transistor characteristics is typically several orders of magnitude larger than the operation cycle period of the circuit. Consequently, an impractically long period of simulation time would be necessary to account for the dynamic aging of MOS transistors within the circuit. An earlier attempt to overcome this problem was to estimate the initial degradation of each transistor, based on a one-cycle circuit simulation, and then to extrapolate the projected degradation assuming that the operating conditions of the transistors remain unchanged [12],[15]. This assumption can certainly not be justified for the general case in which the gradual degradation of device characteristics causes the terminal voltage waveforms of all transistors to change over time. In the following, our proposed solution to this problem will be presented as an integrated simulation framework, which combines the various model components examined in Section I.

It was already pointed out that the use of the device degradation models must be restricted to short time intervals in which the change of stress conditions may be neglected. The simulation of device degradation over longer time intervals can thus be accomplished by periodically updating stress conditions at short intervals, and by repeating the simulation with the new stress conditions. To illustrate this scheme, a step-by-step procedure will be summarized below. It is assumed that the degradation models can be applied to predict the hot-carrier-induced device degradation accurately within a time interval of length T_1. The goal is to predict the amount of device and circuit performance degradation for the operation time

interval $T_2 > T_1$. The period of the input waveform is assumed to be $T_0 \ll T_1, T_2$.

Simulation Procedure:

(i) Simulate the circuit for one period (T_0) and determine the stress conditions (terminal voltage waveforms) associated with each nMOS transistor.

(ii) Using the hot-carrier degradation models, determine the amount of degradation that each transistor will experience at the end of the time interval T_1.

(iii) Update the damage parameters of each transistor to specify the hot-carrier degradation sustained at the end of T_1.

(iv) Return to (i) and repeat the procedure k times such that $T_2 = k\ T_1$.

The major steps involved in this simulation procedure are shown in Fig. 2 [23]. It can be seen that the results of each circuit simulation cycle (for one period T_0) are used to estimate the amount of hot-carrier-induced damage each transistor will experience during a time interval of length T_1. The proposed reliability simulation tool, which has been designed to automatically carry out this procedure, consists of various components combined into a single device model. In the following, the internal structure of the simulation tool will be examined.

The damaged MOSFET model proposed earlier is the central element of the model structure [17],[22]. The model uses a realistic oxide-interface charge distribution profile to account for the localization of hot-carrier damage near the drain. Given the amount of hot-carrier-induced damage and the terminal voltages, this model is capable of accurately representing the current-voltage characteristics of the locally damaged nMOS transistor. The model also replicates the strong asymmetry between the forward and the reverse operations, which is due to

the localization of oxide-interface damage near the drain. The oxide damage in each transistor can be specified by setting only a few physical parameters of the damaged transistor model, namely, the amount of N_{it} and N_{ox}. In the conventional MOSFET models, the effects of such localized oxide damage can only be represented by modifying a large number of model parameters. As a result, previous reliability simulation approaches required extensive updating of most device parameters for this task [15],[24]. The capability to simulate damaged transistors without extensive parameter extraction before and after hot-carrier stress is especially valuable for the overall simplicity of the proposed simulation tool.

To facilitate simple transfer and updating of the damage parameters N_{it} and N_{ox}, these parameters are represented by internal node voltages V_{it} and V_{ox} within the simulation model. Obviously, the voltage values V_{it} and V_{ox} must be determined prior to each circuit simulation cycle, and must be held constant during the simulation period T_0. Once the circuit simulation for one period is completed, these voltages have to be re-evaluated to represent the increased damage level of the transistor. To illustrate the scheme by which the internal node voltages representing the damage are evaluated, the calculation of V_{it} will be considered in the following.

It was explained in Section I that given the average value of the bond-breaking current $\langle I_{BB} \rangle$ over one period, the interface trap density N_{it} at any time point $0 \le t \le T_1$ is found by solving Eq. (17). To calculate the average value of I_{BB} during the simulation, a simple circuit representation is used: The terminal current of a linear capacitor with capacitance value $C = T_0$ is set equal to I_{BB} during the cycle period of length T_0. Since the circuit simulation routine determines the solution for this internal node at each time step, the terminal voltage of the capacitor at the end of the period ($t = T_0$) will correspond to the average bond-breaking

current $\langle I_{BB} \rangle$.

Under a mild assumption[1] that the stress conditions, and consequently $\langle I_{BB} \rangle$, do not change significantly during the time interval T_1, the exact solution of Eq. (17) can be found as:

$$N_{it} + \frac{B_p X_H}{2 D_H} N_{it}^2 = K \langle I_{BB} \rangle t$$

The amount of degradation at the end of a time interval T_1 can thus be found by setting $t = T_1$ and solving the quadratic equation above. This solution is valid for the first iteration with the initial condition N_{it} equal to zero. For the subsequent iterations over equal time intervals T_1, it can be shown that the right-hand side of the equation above is modified as follows.

$$N_{it} + \frac{B_p X_H}{2 D_H} N_{it}^2 = T_1 K \sum_i \langle I_{BB} \rangle^i \qquad (18)$$

Here, $\langle I_{BB} \rangle^i$ denotes the average bond-breaking current calculated during the i_{th} cycle.

The equivalent circuit diagram corresponding to this model is given in Fig. 3. Here, the current source f_1 represents the the drain current simulated by the damaged transistor model. Note that f_1 is a function of the MOSFET terminal voltages, as well as of the internal voltages V_{it} and V_{ox}. The current source f_2 corresponds to the bond-breaking current generated by impact ionization. The nonlinear voltage source f_3 determines the explicit solution of Eq. (18) by using the average voltage V_{avg} as the dependent variable, i.e., its constitutive relationship is

[1]This assumption is used mainly for computational efficiency. Without this assumption, the solution of Eq. (17) would require the numerical evaluation of $\langle I_{BB} \rangle = f(N_{it})$, which would significantly increase the simulation time.

described as follows.

$$f_3\left[V_{avg}\right] = \frac{\sqrt{1 + 2\,T_1\,K\left[\frac{B_p\,X_H}{D_H}\right]V_{avg}} - 1}{\left[\frac{B_p\,X_H}{D_H}\right]} \tag{19}$$

It must be noted that the V_{avg} corresponds to the accumulated average bond-breaking current $\sum_i \langle I_{BB}\rangle^i$ during dynamic operation. Finally, the capacitor C_s is used to store the result. The intermittent value of interface trap density N_{it} is represented by the capacitor voltage V_{it}, and is being held constant during the course of one-cycle simulation. Between two consecutive simulation cycles, the switch is turned on, thus allowing the new updated value of V_{it} to be stored in the capacitor C_s.

The composite degradation model described above is implemented for each transistor in the circuit. Using a simple scheduling scheme, the evaluation of average bond-breaking current $\langle I_{BB}\rangle$, calculation of N_{it} and automatic updating of damage parameters for each transistor can be repeated several times within a single simulation run. Note that each transistor within the circuit will have a unique set of model parameters after undergoing circuit degradation, due to different degradation levels. The user does not need to keep track of various devices and their damage levels, and the long-term simulation of hot-carrier induced device degradation can be accomplished in one simulation run. This implementation also demonstrates the flexibility of the damaged transistor model which is capable of representing the hot-carrier induced damage by only a few parameters. All components of the reliability simulation tool described above have been integrated into a single device model, which has been implemented for the general-purpose circuit simulation program iSMILE [26].

One important aspect of the long-term simulation approach presented in this section is the selection of time interval length T_I, which determines the parameter updating frequency during reliability simulation. The length of the time interval T_I is chosen such that the stress conditions do not change significantly over this time interval. This requirement ensures that the hot-carrier-induced degradation of the devices can be accurately estimated using the quasi-static simulation approach during T_I. If operating conditions of the transistors change during this time period, the simulation results may overestimate or underestimate the actual device degradation. The following simple guideline derived from our simulation studies can be used for the selection of the updating time interval length T_I: Given the interval length, if the change of oxide charge density associated with all transistors within one interval step remains less than 2×10^{11} cm^{-2}, then the interval length T_I is acceptable for sufficient accuracy. The basis for the simple guideline stated above is that most transistor current characteristics exhibit almost negligible degradation for any amount of oxide damage less than 2×10^{11} cm^{-2}. Thus, the operating conditions of all transistors remain essentially unchanged, provided that the damage level of all transistors is below this limit.

C. Circuit Simulation Examples

The applications of the long-term dynamic simulation approach will be illustrated by various examples in the following. In the first simulation example, the hot-carrier-induced degradation of the nMOS transistors in a 7-stage CMOS inverter chain circuit is examined (Fig. 4). The circuit consists of a cascaded connection of seven CMOS inverter stages, each with a W_P/W_N ratio of 15/10. The load capacitance of each intermediate stage is 0.5 pF, and the output load capacitance of the final stage is 0.7 pF. The power supply voltage of the cir-

cuit is $V_{DD} = 5$ V. The circuit is driven with a periodic pulse waveform with rise time $\tau_{rise} = 2$ ns, fall time $\tau_{fall} = 2$ ns, and with a duration $\tau_{high} = 12$ ns.

Figure 5 shows the input and output voltage waveforms of the first stage, and the voltage V_{it1} which represents the amount of degradation experienced by the first stage nMOS transistor. Degradation of the nMOS transistor occurs almost exclusively during the rising input phase. The gradual increase of V_{it1} exhibits a saturating behavior as expected. The hot-carrier-induced degradation of the nMOS transistors is estimated for a time interval of 10^6 sec based on the simulation results for one cycle period ($T_0 = 30$ ns). The damage parameters are automatically updated at the end of each cycle, and the simulation is continued for a total of 16 cycles, which corresponds to a long-term operation of 16×10^6 sec.

The accumulation of hot-carrier-related damage in three selected nMOS transistors is plotted as a function of time in Fig. 6. It can be seen that the expected degradation of Stage 1 is larger than the other two stages plotted here. The reason for this difference is that the input slew rate of Stage 1, which is determined by the externally applied pulse waveform, is less than the slew rates experienced by the subsequent stages. The hot-carrier induced degradation becomes smaller with shorter input signal rise times, since in this case, the nMOS transistor will get out of the saturation region faster. This issue is further examined in Section IV of the report. As the nMOS transistors in the circuit experience parameter degradation, the circuit performance also deteriorates accordingly. The gradual increase of the average delay time of the inverter chain circuit is shown in Fig. 7. The amount of delay time increase is approximately 4 percent over the operating time of 16×10^6 sec.

In the next example, the hot-carrier-induced degradation of a two-input CMOS NAND gate (Fig. 8) will be examined. The nMOS transistors M1 and M2 each have a (W/L)-ratio of 20/1, and the pMOS transistors have a (W/L)-ratio of 15/1. The load capacitance C_L is 1.0 pF, and the combined parasitic junction capacitance C_P is 0.01 pF. The circuit is driven with two periodic pulse waveforms with rise time $\tau_{rise} = 2$ ns, fall time $\tau_{fall} = 2$ ns, and with a duration $\tau_{high} = 12$ ns. Simulation results indicate that the upper nMOS transistor (M1) experiences significant hot-carrier-induced degradation during turn-on, and that the amount of degradation depends largely on the relative timing of rising input signals.

Figures 9(a) and 9(b) show the input and output voltage waveforms of the NAND gate with a positive and a negative input skew, respectively. It is seen that the intermediate node voltage (thin dashed line) rises quickly in case (a) when M1 is turned on, because of charge sharing between the capacitances C_P and C_L. In case (b), however, the capacitance C_P is discharged first when M2 is turned on. Thus, with positive input skew (V_{in1} rises before V_{in2}), the voltage across the source and drain of M1 is reduced very quickly, whereas with negative input skew (V_{in1} rises after V_{in2}), the relatively large load capacitance sustains a large voltage drop across M1 for a longer time during turn-on. The hot-carrier-induced degradation characteristics of M1 for three different input skew conditions are shown in Fig. 10. It is seen that the upper nMOS transistor experiences approximately twice as much damage in the negative skew condition than in the positive skew condition. The variation of hot-carrier-induced damage in M1 as a function of input signal skew is shown in Fig. 11. A small shift in the input skew causes a very significant change in the long-term degradation characteristics, which indicates a high sensitivity of hot-carrier-induced degradation level with respect to the circuit operating conditions.

This property of the NAND2-gate degradation characteristics will be further illustrated in the following example. The upper input of the CMOS NAND2 gate shown in Fig. 8 is driven by the output signal of the 7-stage inverter chain circuit (Fig. 4), while the lower input of the NAND gate is driven by an external signal source. The input signals to the inverter chain circuit and to the lower transistor of the NAND gate (M2) are initially aligned so that the inverter chain output starts rising 0.2 ns before the lower input. Thus, the initial degradation of the upper transistor (M1) of the NAND gate is relatively small. However, as time progresses, the delay time of the inverter chain circuit, which is connected to the upper input terminal (V_{in1}) of the NAND gate, starts increasing, as shown in Fig. 19. The amount of hot-carrier-induced degradation experienced by M1 increases accordingly, as the signal skew between the two inputs of the NAND gate becomes smaller. The hot-carrier-induced degradation in M1 as a function of time is shown in Fig. 12.

Because of the high sensitivity of the degradation level to the operating conditions, the accumulation of damage in M1 cannot be accurately predicted by a one-step simulation method. To illustrate this point, the degradation of M1 is estimated for the time interval of 16×10^6 sec, using only the initial one-cycle simulation results (Fig. 12). The one-step quasi-static simulation approach significantly underestimates the hot-carrier-induced degradation in M1.

III. A PROBABILISTIC TIMING APPROACH TO HOT-CARRIER EFFECT ESTIMATION

Recently, we have used timing simulation for hot-carrier effect (HCE) estimation [27],[28]. The approach in [27] employs fast-timing simulation to simulate subcircuits with no damage and detailed circuit simulation to estimate HCE in the damaged subcircuits. In [28], a macromodel of channel-connected MOS blocks is constructed and fast timing simulation is used to predict the degradation effects over time. In both of these approaches deterministic simulation is used, and the most damaged subcircuit/transistor is obtained assuming that a user-specified input waveform is continuously applied to the circuit. Since HCE is a long-term process, the combined effects of many input waveforms have to be applied before the characteristics of some transistors degrade sufficiently to affect the performance of the entire circuit. To determine the most damaged transistor with respect to all of the possible input waveforms, exhaustive simulation or at least a large number of simulations, such as in Monte Carlo techniques, have to be done to predict HCE.

In this part of the work, we combine the timing and the probabilistic simulation techniques [29] to estimate HCE in a single simulation run. When statistical descriptions of primary input signals are given, the probabilistic timing simulation uses statistical techniques to obtain the corresponding statistical descriptions of voltage and current waveforms inside the circuit. From the data of voltage and current waveforms, the expected degradation of each transistor is calculated to pinpoint the most critical transistor(s).

A. Hot-Carrier Effects

Experimental formulas have been derived for estimating HCE [6],[22],[31],[32], as explained in the previous sections. To estimate the relative HCE damage in each transistor, the following equations are used to calculate the substrate current I_{SUB}, the bond-breaking current I_{BB}, and the interface states N_{it} [34]:

$$I_{DS} = k_p \frac{W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad \text{for } 0 \le V_{GS} - V_T \le V_{DS} \tag{20}$$

$$I_{DS} = k_p \frac{W}{2L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad \text{for } 0 \le V_{DS} \le V_{GS} - V_T \tag{21}$$

$$V_{DSAT} = \frac{E_{crit0}L(V_{GS} - V_T)}{E_{crit0}L + V_{GS} - V_T} \tag{22}$$

$$I_{SUB} = \frac{A_i}{B_i} I_{DS} (V_{DS} - V_{DSAT}) \exp\left[\frac{-B_i l_c}{V_{DS} - V_{DSAT}}\right] \tag{23}$$

$$I_{BB} = \frac{I_{SUB}^{\alpha}}{I_{DS}^{\beta}} \tag{24}$$

$$N_{it} + \frac{B_p X_H}{2D_H} N_{it}^2 = \int_0^T K\, I_{BB} dt \tag{25}$$

where $\alpha = 2.9$, $\beta = 1.9$; $E_{crit0} = 10^4$ V/cm; D_H and X_H represent diffusion constants; K and B_p represent process-dependent coefficients; and $l_c = 0.2X_{ox}^{1/3}X_j^{1/2}$, where X_{ox} is the oxide thickness and X_j is the junction depth. From the equations above, it can be observed that I_{SUB} is the key factor in estimating the interface states.

Figure 13 illustrates the relation between V_{in}, V_{out}, I_{DS}, and I_{SUB} of the nMOS transistor of a typical CMOS inverter obtained using *SPICE*. Two main factors, in addition to the feature size, may affect the magnitude and time span of I_{SUB}: (i) The switching frequency of the nMOS transistor; it follows that the higher the switching frequency, the more damage the transistor experiences; and (ii) the duration a transistor stays in the saturation region, which depends on the input slew rate and the loading capacitance. A slower slew rate causes a longer I_{SUB} time span and, hence, more degradation, and a higher loading capacitance also results in longer time in saturation.

After performing detailed circuit simulation to obtain accurate HCE estimation of a CMOS inverter circuit, we have found that, by approximating V_{out} in Fig. 13(a) with a ramp as drawn in Fig. 13(b), the error of the I_{SUB} peak value is less than 2%. Thus, ramp approximation to the voltage waveforms is used during transition.

B. Probabilistic Voltage Waveform Description

As shown in Fig. 14, an event is defined as a switching of voltage waveforms with non-zero probability. For an event occurring at time t_0, five values have to be specified: $Ph(t_0^-)$, $Ph(t_0^+)$, $Plh(t_0)$, $t_{LH}(t_0)$ and $t_{HL}(t_0)$, where $Ph(t_0^-)$ is the probability of the signal being high right before t_0, $Ph(t_0^+)$ is the probability of the signal being high right after t_0, $Plh(t_0)$ is the probability of the signal switching from low to high, and $t_{LH}(t_0)$ and $t_{HL}(t_0)$ are the low-to-high and high-to-low transition times of the input signal. If there is a complete transition, then the actual voltage waveform (a ramp) can be reconstructed as

$$V(t) = \begin{cases} 5 * \left[\dfrac{t - t_0}{t_{LH}} \right] & \text{when } V(t_0^-) = 0,\ t_0 \le t \le t_0 + t_{LH} \\ 5 * \left[1 - \dfrac{t - t_0}{t_{HL}} \right] & \text{when } V(t_0^-) = 5,\ t_0 \le t \le t_0 + t_{HL} \end{cases} \tag{26}$$

The probability Phl(t) can be derived from [29] as

$$Phl(t) = Ph(t^-) + Plh(t) - Ph(t^+). \tag{27}$$

The signal transition times $t_{LH}(t_0)$ and $t_{HL}(t_0)$ are added here to the probabilistic waveform description given in [29] to estimate the HCE more accurately.

During the probabilistic simulation, the expected value of the output statistical information is generated with respect to the input events for each subcircuit, and the output information is used as input events for subsequent fanout subcircuits.

C. Single Gate Simulation

A gate is defined to be a channel-connected subcircuit. The simulation of a single gate consists of two parts: one is steady-state analysis, where Ph(t) at the gate output node before and after switching is obtained from the Ph(t) given at the gate input nodes. Switching analysis involves the computation of Plh(t), Phl(t), $t_{LH}(t)$, $t_{HL}(t)$, and the delay Δt through the subcircuit when an input switches.

The problem of calculating $Ph(t_I^{\pm})$ of the output node is equivalent to finding the probability of having a conducting path from the output node to V_{DD}. i.e.,

$$Ph(t_l^{\pm})_{out} = P_{on}(t_l^{\pm}, e_1 = (out, V_{DD})) = 1 - P_{on}(t_l^{\pm}, e_2 = (out, G_{ND})), \quad (28)$$

where $P_{on}(t^{\pm}, e)$ represents the probability of having a conducting path through edge e before or after t. For series-parallel CMOS circuits without pass transistors, a graph reduction procedure described in [33] is used.

For switching analysis, signals are assumed to switch instantaneously; thus, no two signals switch at the same time [33]. Thus, in a subcircuit only one transistor switches at a given time. It follows then that when an nMOS transistor M_i in a CMOS gate causes a transition, *there exists at least one conducting path from the output node to* G_{ND} *and all of the valid conducting paths must pass through* M_i *[33].* The same requirement holds for pMOS transistors with G_{ND} changed to V_{DD}.

As shown in [29], the switching probability of the output, Phl or Plh, is found by the graph reduction techniques. Here we concentrate on the computation of the expected values of the currents in those transistors next to the output node that are most susceptible to HCE and on the estimation of the delay and the slew rate of the output in relation to the input. We use the macromodeling approach in [29] and [33]. Two types of macromodels shown in Fig. 15 are used. In the first macromodel, shown in Fig. 15(c), all conducting transistors are reduced to equivalent conductances G_n for the nMOS transistors and G_p for the pMOS transistors. The transistor pair connected to the output node through which the current is to be estimated is not reduced. Note that the transistor conductances G_i are random variables and formulas derived in [33] for series and parallel combinations are applied to find the equivalent conductances G_n and G_p, which are also random variables. The second macromodel shown in Fig. 15(d) is derived for each switching transistor that is not connected to the output node; the

reduction is done using the transconductance parameter β ($= k\frac{W}{L}$) of the conducting and the switching transistors. Here β is considered a random variable.

The equivalent conductance G_n (G_p) is the conditional expected value $E[g_e | e \neq 0]$ after the graph reduction, where e is the equivalent edge from the output node to G_{ND} (V_{DD}). The same method can be used to derive the equivalent expected value of the transconductance parameter (β). With the macromodel shown in Fig. 15(c), we have the following differential equations:

$$C_{load}\frac{dV_{out}}{dt} = i_p(V_A, V_2, V_{out}) - i_n(V_A, V_{out}, V_1) \tag{29}$$

$$V_2 = V_{DD} - i_p / G_p \tag{30}$$

$$V_1 = i_n / G_n. \tag{31}$$

When the second macromodel shown in Fig. 15(d) is used, Eqs. (30) and (31) are removed and (29) will include the equivalent expected value of β. As shown in Algorithm 1 below, when the macromodel shown in Fig. 15(c) is used, several inner iterations are necessary to calculate V_1 and V_2 at each time point; but during the outer loop, only equation evaluation is required. The disadvantage of this model (compared with the model in Fig. 15(d)) is the time spent in the inner iterations. However, its advantage is that more accurate voltage and current waveforms across the switching transistor can be obtained.

Algorithm 1. The timing simulation algorithm:

```
for each output transition event_i {
    check if event_i overlaps with event_{i-1};
    set initial value of V_out, V_1, V_2, t = t_0, h (time step);
    while V_out > V_Tn {  /* V_out < V_DD - V_Tn if low_to_high transition */
        t <- t + h
        update V_G;
        using Newton method to calculate V_1 and V_2;
        /* not necessary if employing the macromodel in Fig. 15(d) */
        I_p <- i_p(V_G, V_2 ,V_out); /* eqns. (20), (21) */
        I_n <- i_n(V_G, V_out ,V_1);
        ΔV_out ← (I_p - I_n) h / C_load;
        if ΔV_out > upperbound
            t <- t - h; decrease time step h;
        else{
            V_out ← V_out - ΔV_out;
            If the switching nMOS is at top position
                estimate degradation using V_G, V_out, V_1, I_n, h, and Phl_event_i;
                the degree of overlap is also taken into account.
            if ΔV_out < lowerbound
                increase time step h;
        }
    }
}
```

During the simulation, the following time points have to be computed to estimate the degradation during transition. Here we only consider the switching from high-to-low; the same method can be applied to the low-to-high transition. Figure 16 illustrates the relation between these values. The conventions used in Fig. 16 are described below:

t_a = the time point at which the nMOS transistor starts conducting ($V_{GS}(t_a) = V_{T_n}$).

t_b = the time point at which the output voltage drops to $V_{DD} - |V_{T_p}|$.

t_c = the time point at which the transistor enters the linear region ($V_{DS} < V_{GS} - V_{T_n}$).

t_d = the time point at which the output voltage drops to V_{T_n}.

$$t_{HL} = (t_d - t_b) \frac{V_{DD}}{V_{DD} - V_{T_n} - |V_{T_p}|} \tag{32}$$

$$\begin{aligned} \Delta t &= t_1 - t_0 \\ &= \left[t_b - t_{HL} \frac{|V_{T_p}|}{V_{DD}} \right] - t_0 \end{aligned} \tag{33}$$

Usually the propagation delays of low-to-high and high-to-low transitions are different [30]; this property may result in waveform dispersion. To simplify the problem, the weighted average of the up- and down-transition propagation delays is taken by using their "probability to occur" as weights [29], i.e.,

$$\Delta t_{average} = \frac{\Delta t_{lh} Plh(t)_{out} + \Delta t_{hl} Phl(t)_{out}}{Plh(t)_{out} + Phl(t)_{out}}. \tag{34}$$

In this way, the up- and down-transitions of each event are always bound together after the signal is propagated through the circuit. The output waveform ($Ph(t^-)$, $Ph(t^+)$, $Plh(t)$, $t_{LH}(t)$, $t_{HL}(t)$) then becomes an input to the fanout subcircuits. With Eqs. (20)-(25), (32) and (33), the damage of the switching MOS transistor during the transition can be determined. Here Eq. (25) has to be modified to include the probability Phl_{out}.

$$N_{ii} + \frac{B_p X_H}{2D_H} N_{ii}^2 = \sum Phl_{out} \int_{t_s}^{t_e} K\, I_{BB} dt. \qquad (35)$$

Here $\sum$ is a summation over all of the events that propagate through the switching transistor and cause the output to switch from high to low.

Since the voltage waveform slew rate is included in the waveform specification, overlap during transition could occur and has to be taken into account. If two events are close to each other, there is a certain possibility that one transition occurs before the other transition is completed. We have found that the overlap only affects the drain current of the second transition segment of two overlapped events and, hence, determines the damage during the second transition.

E. Implementation and Simulation Results

The above approach has been implemented in a computer program named *iProbe-d* [38]. The program consists of four main parts: (1) Input circuit reading subroutines, (2) partitioning and scheduling, (3) circuit simulation, and (4) probabilistic and timing simulations.

iProbe-d reads in *SPICE*-type circuit descriptions and creates a circuit database. The circuit can be described hierarchically. Instead of flattening the circuit, this program preserves the circuit hierarchy to save memory space.

iProbe-d has been used to simulate several benchmark circuits. Although the program currently can only simulate series/parallel CMOS circuits, it is being extended to handle general nMOS and CMOS circuits.

Figure 17 shows a CMOS circuit with two NAND gates and one NOR gate; this type of circuit is quite common in two-level logic synthesis. The statistical descriptions of the four input nodes are also shown in the figure. Table I illustrates the degradation of the six nMOS transistors using *iProbe-d*, *SPICE exhaustive simulation*, and *SPICE one run*, respectively. The circuit is simulated for a time period T = 20 ns. It is assumed the input events repeat periodically and the damage is extrapolated to three months. Since for each input node, there are four possible waveforms (staying high, staying low, switching from low to high, from high to low), there are $4^4 = 256$ possible input combinations. Therefore, for the *SPICE exhaustive simulation*, 256 runs are needed. On the other hand, only one run is necessary when *iProbe-d* is employed. The input voltage waveforms of the third row in Table I, *SPICE one run*, are $A = B = D = V_{DD}$ *and* $C =$ *a periodical square wave*. From the result, *iProbe-d* and *SPICE exhaustive simulation* show the same tendency, while running *SPICE* with one particular input waveform points to the wrong critical transistor. We have also compared the waveforms obtained from *iProbe-d* and *SPICE exhaustive simulation*. The slew rate and propagation delay from *iProbe-d* are within 5% error compared to the average value from *SPICE exhaustive simulation* on all of the output nodes.

	NAND1 top	NAND1 bottom	NAND2 top	NAND2 bottom	NOR left	NOR right
SPICE exhaustive						
τ = *5ns*	1.178	0.012	1.177	0.022	1.963	1.898
τ = *2ns*	1.178	0.012	1.177	0.399	1.741	1.197
τ = *1ns*	1.178	0.011	1.177	0.752	1.740	0.876
τ = *0.3ns*	1.178	0.012	1.178	0.015	1.740	0.868
iProbe-d						
τ = *5ns*	1.094	0	1.094	0	2.186	2.173
τ = *2ns*	1.087	0	1.094	0	1.873	1.554
τ = *1ns*	1.094	0	1.094	0	1.795	1.544
τ = *0.3ns*	1.094	0	1.094	0	1.795	1.544
SPICE one run *	0	0	2.442	0	0	5.654

Table I. The damage N_{it}($x10^{11}C/cm^2$) of all the nMOS transistors in the circuit shown in Fig. 17.
* A = B = D = high(V_D); C = a periodical square wave.

Some ISCAS85 benchmark circuits have also been analyzed. These benchmark circuits have been converted to *SPICE* input file with complementary CMOS transistor circuit implementation of each gate. Table II shows the computation time on a SPARC station 2, as well the damage situation after a simulated 3 months of continuous operation. Here we assign one event to each primary input node, with 20 ns as the simulation period. The results show that *iProbe-d* can handle large circuits with reasonable computation time.

ISCAS85 benchmark circuit	# of nMOS transistors in each damage level (Normalized Nit)							Computation time (sec)
	<0.1	0.1 - 1.0	1.0 - 2.0	2.0 - 3.0	3.0 - 4.0	4.0 - 5.0	>5.0	
C432	196	16	52	58	42	16	32	23.87
C499	336	40	48	80	16	56	306	20.75
C880	256	112	103	57	117	115	141	25.14
C1355	512	72	208	16	176	64	106	46.03
C2670	743	95	106	190	440	401	707	77.43

Table II. The computation time of *iProbe-d* on several benchmark circuits, and predicted average damage after 3 months of continuous operation. The simulation is done on a SUN4 SPARC station 2.

IV. PARAMETRIC MACROMODELING OF HOT-CARRIER-INDUCED DYNAMIC DEGRADATION IN MOS VLSI CIRCUITS

Hitherto efforts to evaluate the hot-carrier-induced device degradation in a circuit environment have mostly focussed on the development of circuit-level (SPICE-like) simulation tools [22],[25],[27],[34] on the probabilistic simulation reported in Section II. These reliability simulation tools can be used to evaluate long-term circuit degradation and to improve the reliability by incremental design modifications. However, there is an increasing need for a set of geometry-based design rules to improve long-term reliability that can be readily applied to device and circuit designs.

The extent of the hot-carrier damage that each nMOS transistor experiences during dynamic circuit operation is determined primarily by its terminal voltage waveforms, and it is influenced by such parameters as the gate voltage rise time, drain voltage fall time, channel width, channel length and input signal frequency. The challenges in developing reliability-oriented design rules are to identify a set of relevant device and circuit parameters and to express the hot-carrier-related dynamic degradation of nMOS transistors under circuit operating conditions as a simple function of these design parameters. In this section, a parametric reliability measure is developed for estimating the hot-carrier-induced degradation based on the layout geometry. The macromodel derivation presented here is based on the well-known interface trap generation model [6], and is consistent with degradation models used in most reliability simulators [22],[25],[34]. The analysis results obtained by using the macromodel for various simple circuit configurations agree with recently published experimental findings [35],[36]. The parametric design-for-reliability rules devised in this work can also be used for geometry-based early diagnosis of potential reliability problems in CMOS circuits.

A. Parametric Macromodel

The hot-carrier-related damage in nMOS transistors is caused by the injection of high-energy electrons and holes into the gate oxide near the drain region. The degradation of the I-V characteristics of nMOS transistors in digital logic circuits is attributed primarily to the generation of localized interface traps near the drain [35]. It is well-known that the dynamic behavior of interface trap generation can be described by the following simple power-law expression [34]

$$N_{it}(t) = C \left[t \cdot \frac{1}{T} \int_{t_0}^{t_0+T} I_{BB}(\tau)\, d\tau \right]^n \tag{36}$$

where N_{it} is the interface trap density, C is a process-dependent constant, T is the signal cycle period, and the exponent n is in the range of 0.5 - 1.0. The *bond-breaking current density* I_{BB} is defined as $I_{BB} = (1/W_n)\, I_{SUB}^m / I_{DS}^{m-1}$, where $m = 3$ is used in the following analysis. Since the amount of generated interface trap density N_{it} is a direct indication of the hot-carrier damage experienced by the nMOS transistor, the average bond-breaking current density $\langle I_{BB} \rangle$ over a one-cycle period provides an accurate measure of the dynamic device degradation. (Although the substrate current I_{SUB} was long regarded as an indicator of hot-carrier damage in nMOS transistors, the quantity I_{SUB}^m / I_{DS}^{m-1} has been shown to be a better measure of the interface trap generation process responsible for degradation [6],[34],[36].) Note that the enhancement of nMOS device degradation reported for dynamic operating conditions will not be considered in the following analysis. The enhanced dynamic degradation has been linked to hot-hole injection into the gate oxide, a mechanism which is not pronounced in circuits operating with a

power supply voltage $V_{DD} \leq 5V$, as in most CMOS VLSI circuits. Also, the relatively less significant degradation of pMOS transistors is neglected in the following analysis.

The extent of the hot-carrier damage that each transistor experiences is dictated by the operating conditions of the circuit. The resulting degradation of device characteristics also leads to the degradation of circuit performance over time [36],[37]. The aims of the following analysis are to identify the significant circuit parameters influencing the hot-carrier-related degradation and to devise simple macromodels for parametric evaluation of hot-carrier reliability in various circuit structures.

A.1. Degradation of CMOS inverters

In CMOS inverter circuits driven by a ramp-input, hot-carrier-induced damage occurs primarily during the rising-input transient, when the nMOS transistor operates in saturation [37]. A simple CMOS inverter is shown in Fig. 18 along with typical input and output voltage waveforms, as well as the corresponding bond-breaking current waveform. Let the input voltage be a ramp function, $V_{GS}(t) = at + V_T$, where a represents the input slope and is defined as $a = \Delta V/\tau_{rise}$. The influence of MOS oxide and junction capacitances and of external line capacitances upon the dynamic behavior can be represented with sufficient accuracy by a lumped capacitance C_L at the output node of the inverter. For development of macromodels, the channel current I_{DS} of the nMOS transistor is represented by using the well-known Shichman-Hodges model, and the substrate current is calculated using the model devised by Hu *et al.* [34]. When the nMOS transistor is in saturation, the bond-breaking current density can thus be expressed as a function of

$$I_{BB}(t) = K_1 (at)^2 \left[V_{DD} - \frac{1}{3} K_3 \frac{W_n}{C_L} a^2 t^3 - at \right]^3 \exp \left[\frac{-K_2}{V_{DD} - \frac{1}{3} K_3 \frac{W_n}{C_L} a^2 t^3 - at} \right] \qquad (37)$$

where K_1 and K_2 represent process-dependent constants, and $K_3 = \mu_n C_{ox}(1/L)$. It is seen that the *average* bond-breaking current density $\langle I_{BB} \rangle$ over one period (T) is found to be a function of only two designable circuit parameters, a and (W_n/C_L).

$$\langle I_{BB} \rangle = \frac{1}{T} \int_0^T I_{BB}(t)\, dt = f\left[a\ ,\ W_n/C_L \right]. \qquad (38)$$

An interesting result of Eq. (37) is that the amount of dynamic degradation, i.e., $\langle I_{BB} \rangle$, depends on the *ratio* of (W_n/C_L), and not individually on W_n and C_L. Note that the input slope a is primarily determined by the (W_p/C_L) ratio of the *previous* inverter stage, which drives the inverter under consideration. Equation (37) can also be used to evaluate the influence of the power supply voltage V_{DD} and of the nMOS transistor channel length L upon dynamic degradation. For a comparative analysis of the device degradation levels in a given circuit, however, both of these quantities may be assumed to be constant. Figure 19 shows the expected degradation $\langle I_{BB} \rangle$ of the nMOS transistor in a CMOS inverter circuit as a function of input signal slope a and the ratio (W_n/C_L), according to the macromodel. The range of signal slope values is between 1 V/ns and 10 V/ns, and the range of (W_n/C_L) values is between 2 μm/pF and 20 μm/pF. It can be observed that $\langle I_{BB} \rangle$ increases with decreasing a and with decreasing (W_n/C_L). The degradation becomes significantly smaller with shorter input signal rise time, since in this case, the nMOS transistor will get out of the saturation region faster. Figure 19 also shows that the influence of the input signal slope a upon degradation is stronger than that

of (W_n/C_L).

The results of a series of dynamic degradation experiments using CMOS inverter chains have been reported recently by Weber *et al.* [35],[36]. It was found that for CMOS inverters, the influence of the capacitive load on the degradation is relatively small. On the other hand, the degradation was shown to be a relatively strong function of the rising gate voltage slope [36]. The results obtained from the simple expression (37) given above agree with these recent findings.

The developed macromodel can thus be used for deriving the following simple design-for-reliability rules for CMOS inverters:

(i) Smaller input signal rise time leads to less degradation : $\langle I_{BB} \rangle \propto 1/a^{0.8}$;

(ii) Larger (W_n/C_L) ratio leads to less degradation : $\langle I_{BB} \rangle \propto 1/(W_n/C_L)^{0.3}$.

Note that the output voltage rise time and, hence, the pMOS transistor size of the *previous* stage are important design considerations for long-term reliability, because of the strong influence of input rise time upon dynamic degradation. Since the hot-carrier-related degradation occurs only during the rising input transient, the amount of degradation in a certain time period must be related to the number of switching events during that time period. For a comparative evaluation of long-term device reliability in a circuit environment, it may be assumed that all gates under investigation have the same input switching rate, which in fact is a worst-case approximation.

A.2 Degradation of scaled inverter chains and logic circuits

In scaled CMOS inverter chain circuits, the nMOS and pMOS transistor W/L-ratios of each inverter stage are F times larger than that of the preceding inverter, so that the inverter stages have progressively larger current driving capability. Since the W_n/C_L and W_p/C_L ratios remain the same for each scaled inverter stage, each nMOS transistor in the chain experiences approximately the same amount of hot-carrier degradation. At the same time, the *amount* of degradation is a linear function of the scaling factor F. Thus, an inverter chain designed with a smaller scaling factor, i.e., with a larger number of stages, is expected to be more reliable than an inverter chain designed with a larger scaling factor.

In CMOS NOR gates, only the nMOS transistor with the earliest arriving rising input voltage will experience significant hot-carrier-related degradation, since the other parallel transistors with later arriving inputs will not operate in deep saturation due to the already reduced drain voltage. The expressions derived for the degradation of CMOS inverters above can thus be used for NOR gate structures by modifying the equivalent channel width W_n. In CMOS NAND gates, only the uppermost nMOS transistor in the series structure experiences hot-carrier-induced degradation during rising input. The degradation is found to be significantly larger for the case in which the uppermost input arrives later than the lower inputs. It can be shown that the degradation of the uppermost nMOS transistor can be estimated as a function of input signal slope a and the (W_n/C_L) ratio with Eq. (36) by setting its source voltage to approximately 0.2 V. This approach departs slightly from the $V_S = 0$ V approximation proposed by Weber *et al.* [35],[36], and was shown to produce more accurate damage estimates.

A.3 Degradation of nMOS pass gates

In nMOS pass-gate circuits (Fig. 20), the transistor experiences significantly more hot-carrier damage during the *charge* phase than during the *discharge* phase [37]. Assuming that the drain voltage of the pass-gate transistor is constant (V_{DD}), and that the gate voltage is a ramp function with slope a during the charge-up phase, the change of the source voltage V_S can be described as a simple function of time, the gate voltage slope a, the total lumped capacitance C_L being charged up through the pass gate, and the pass-gate transistor size, W_n. The bond-breaking current density, which will be used as a measure of hot-carrier damage in the pass-gate transistor, is derived to be

$$I_{BB}(t) = K_1 (V_{DD} - at)^3 \exp\left[\frac{-K_2}{V_{DD} - at}\right] \left[\sqrt{\frac{a\,C_L}{W_n\,K_3}} \frac{\exp\left[-2t\sqrt{\frac{a\,W_n\,K_3}{C_L}}\right] - 1}{\exp\left[-2t\sqrt{\frac{a\,W_n\,K_3}{C_L}}\right] + 1}\right]^2 . \qquad (39)$$

The hot-carrier-induced damage $\langle I_{BB} \rangle$ during the charge-up phase can again be described by a parametric closed-form expression, which is a function of the input signal slope a and the (W_n/C_L) ratio.

Figure 21 shows the expected degradation of the nMOS pass-gate transistor as a function of a and (W_n/C_L). Unlike the CMOS inverter case, the input signal slope is found to have negligible influence upon the degradation characteristics, whereas larger (W_n/C_L) ratios lead to significantly less degradation of the nMOS transistor.

V. SUMMARY

During the 1991-92 project period, we have developed accurate models and simulation tools for predicting degradations in gate oxides and circuit performances of CMOS VLSI chips, in particular, the simulation of gate-oxide degradation during long-term circuit operation and the simulation of circuit performance degradation after hot-carrier stress. Building on such models, we have also developed computationally efficient methods for probabilistic simulation of hot-carrier effects by applying the probability models of circuit switching and delays. The *iProbe-d* program, which implements the new algorithm and hot-carrier-damaged transistor models, has been shown to simulate the hot-carrier effects with high computational efficiency; a single run of *iProbe-d* provides as much information as exhaustive runs of SPICE-like simulators.

Also reported are new parametric macromodels aimed for development of a reliability rule checker. The parametric macromodels can predict the level of hot-carrier damages in logic gates from the geometrical data of the circuit, namely, the ratio of the n-channel transistor size (W_n) and the load capacitance (C_L) and the input slew rate (a) which can be determined from the pull-up p-channel tree and the parasitic capacitance driven by the p-channel tree. It has been shown that the qualitative behaviors of these parametric macromodels match well with the reported experimental data.

The accomplishments in this project period will form the basis in the development of reliability rule checking CAD tools. Preliminary test results have been encouraging in view of the fact that even very large circuits containing hundreds of thousands of transistors can be analyzed for hot-carrier damages in tens of minutes, which has not been possible with the simulation techniques.

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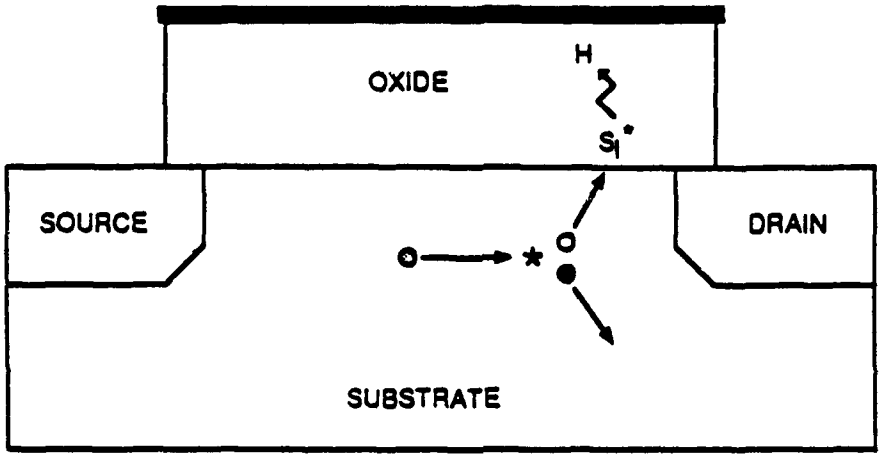


Fig. 1. Interface trap generation through hydrogen bond breakage.

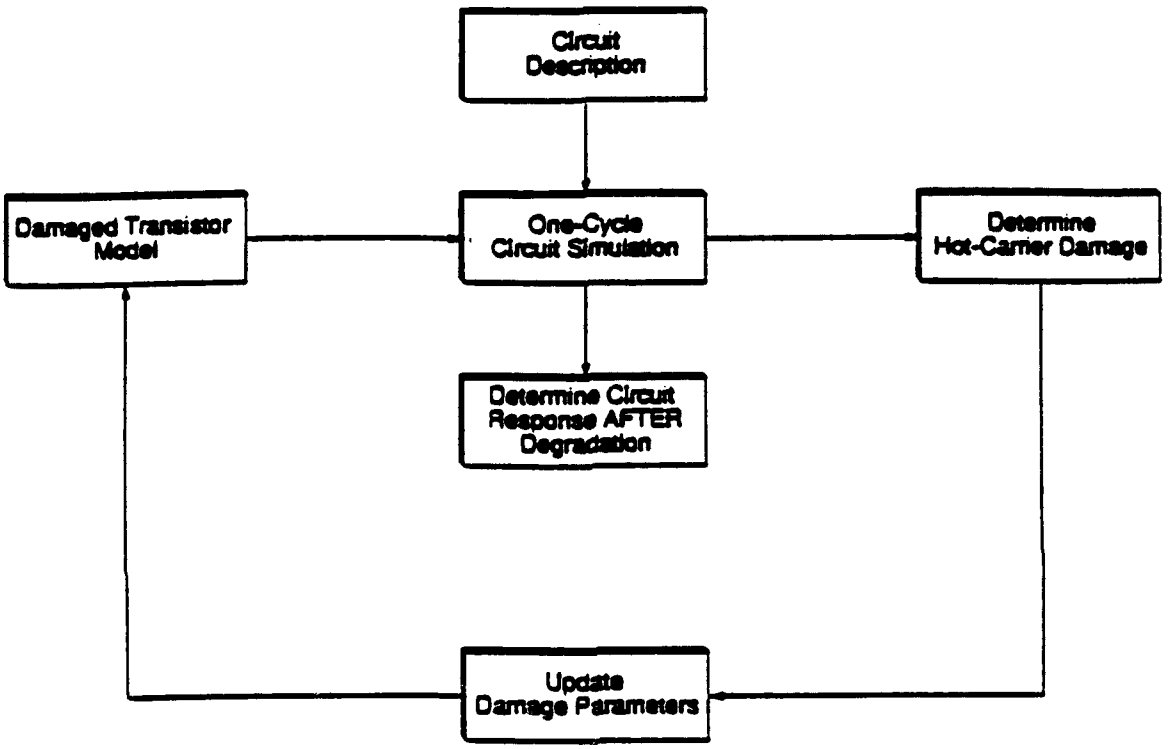


Fig. 2. The major steps of the long-term reliability simulation procedure.

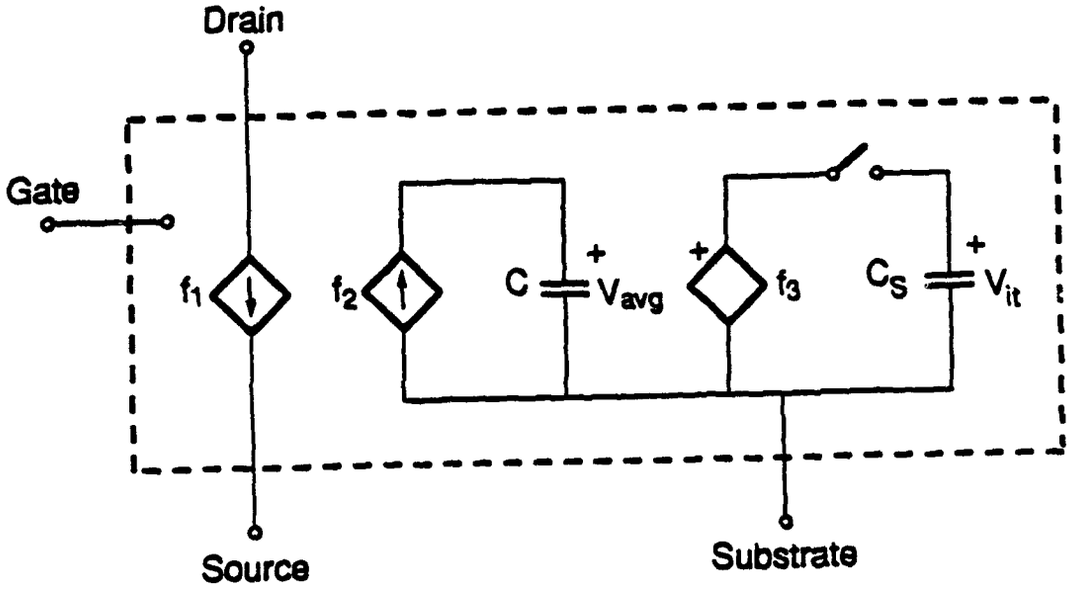


Fig. 3. Equivalent circuit diagram of the model presented in Section II.

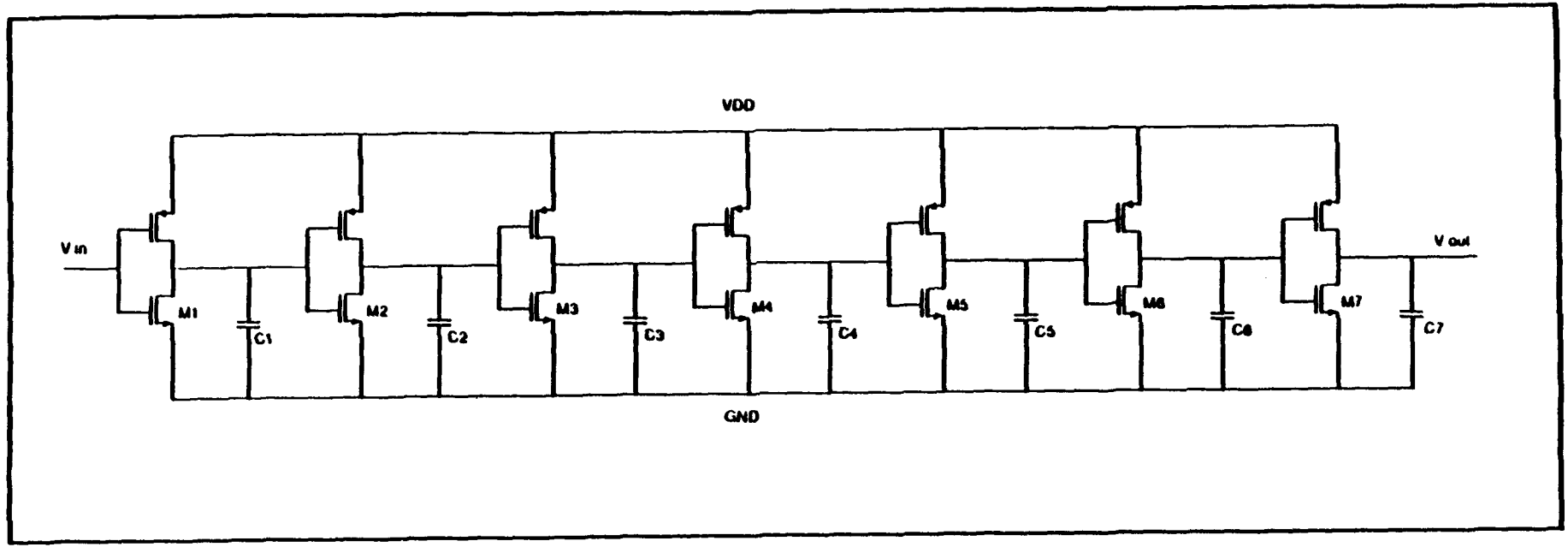


Fig. 4. Seven-stage CMOS inverter chain circuit.

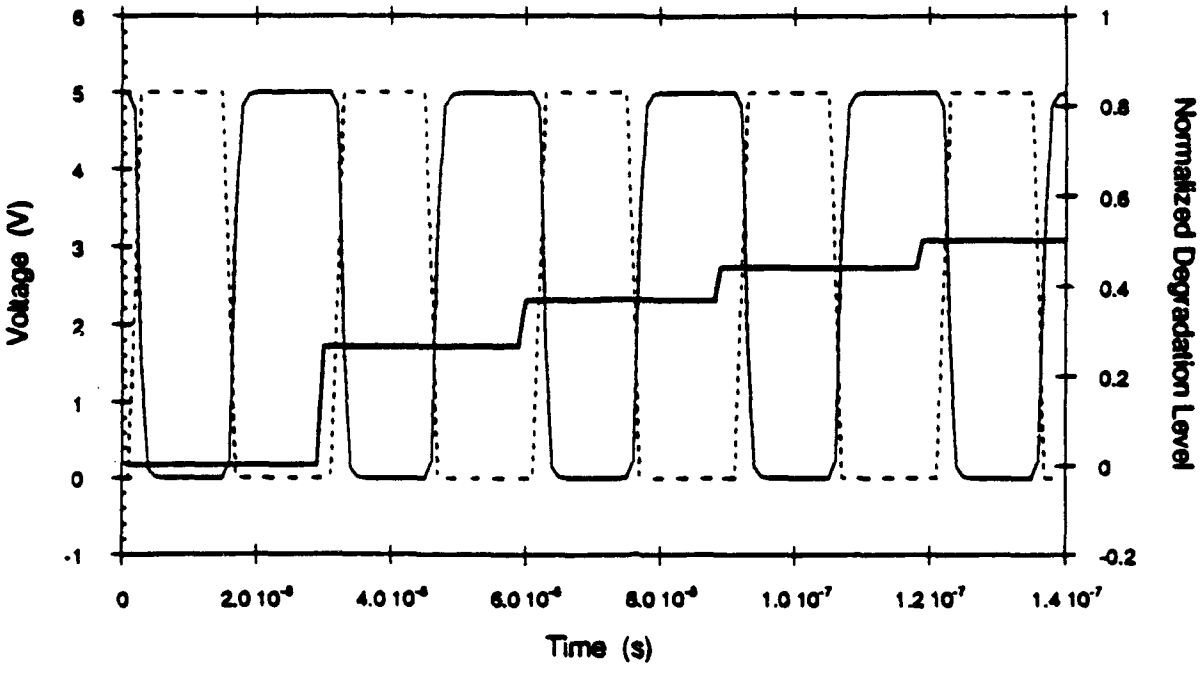


Fig. 5. Input (dashed line) and output (thin solid line) voltage waveforms of the first CMOS inverter stage, and the simulated degradation of the first-stage nMOS transistor v_{it1} (thick solid line).

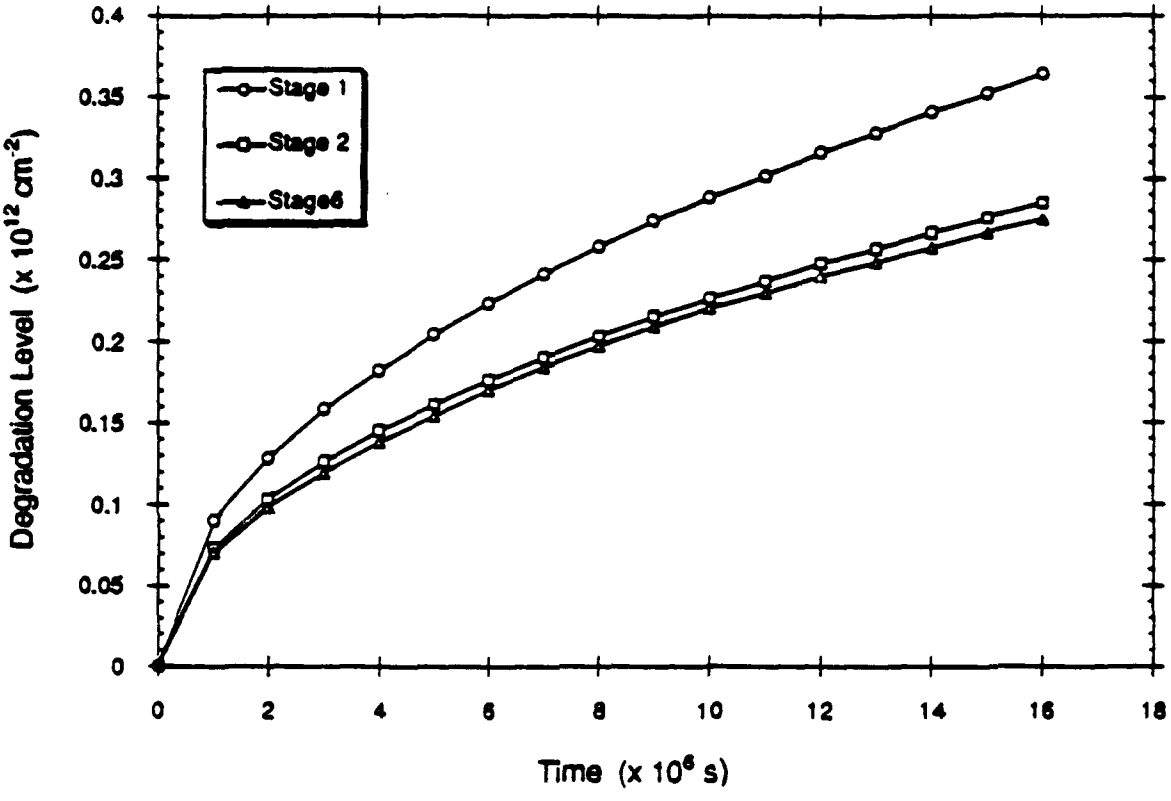


Fig. 6. Simulated degradation versus operation time for three selected inverter stages of the seven-stage CMOS inverter chain circuit.

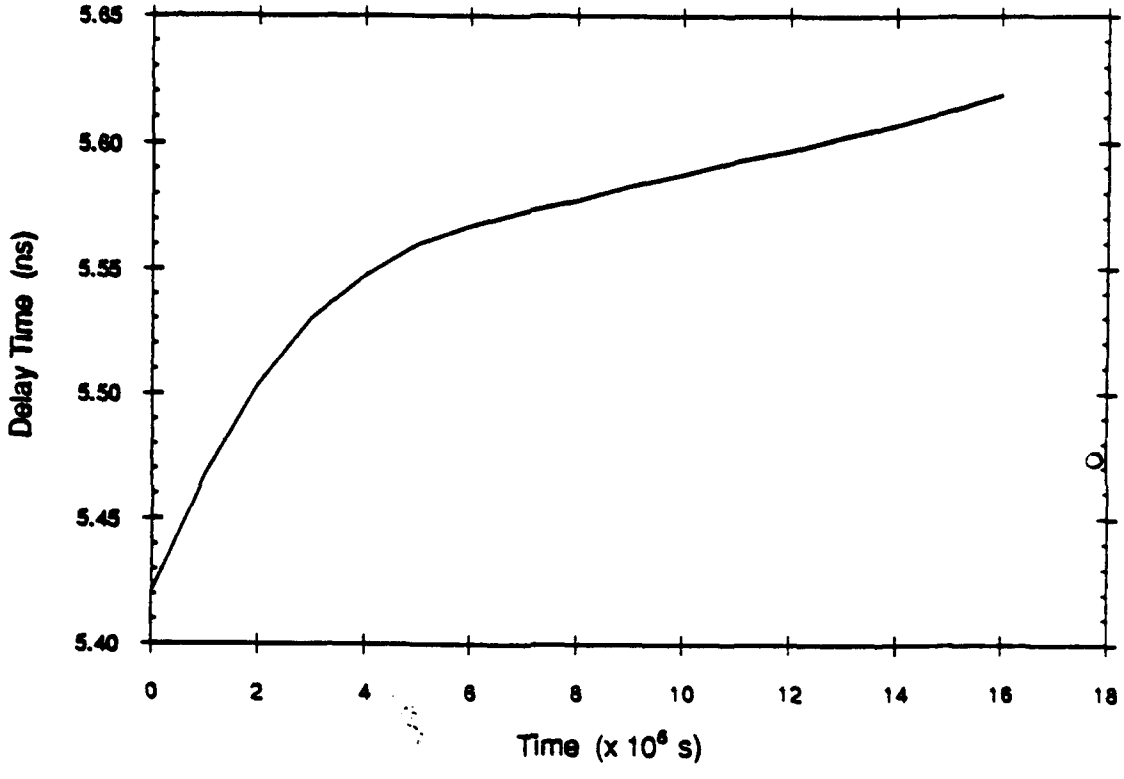


Fig. 7. The average propagation delay time of the seven-stage CMOS inverter chain circuit versus operation time.

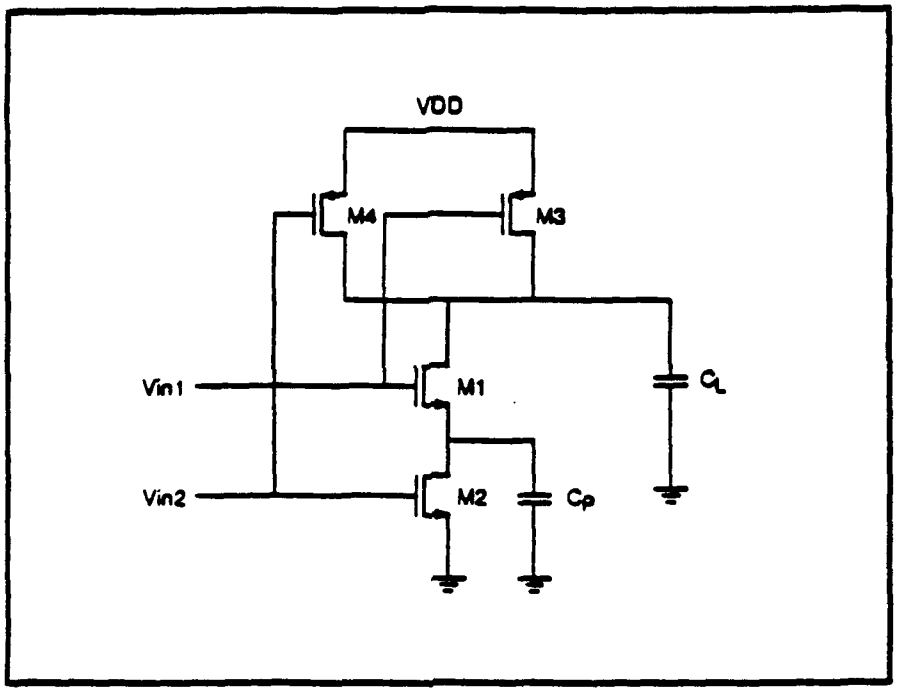
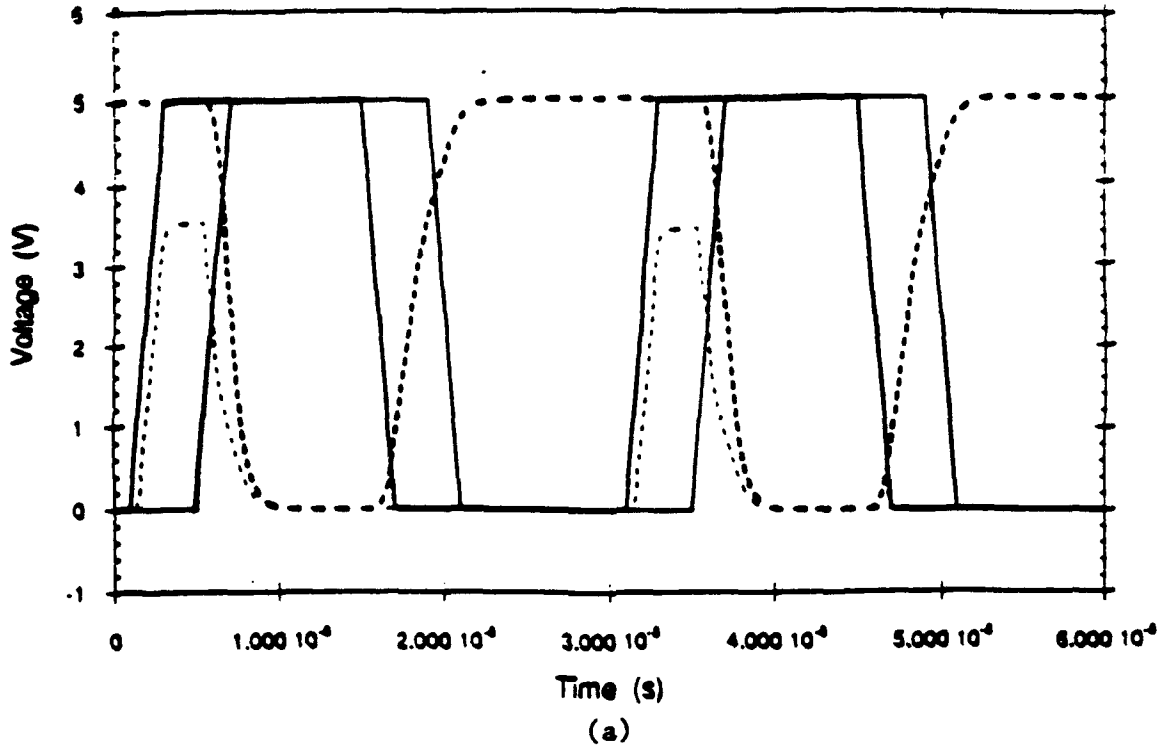
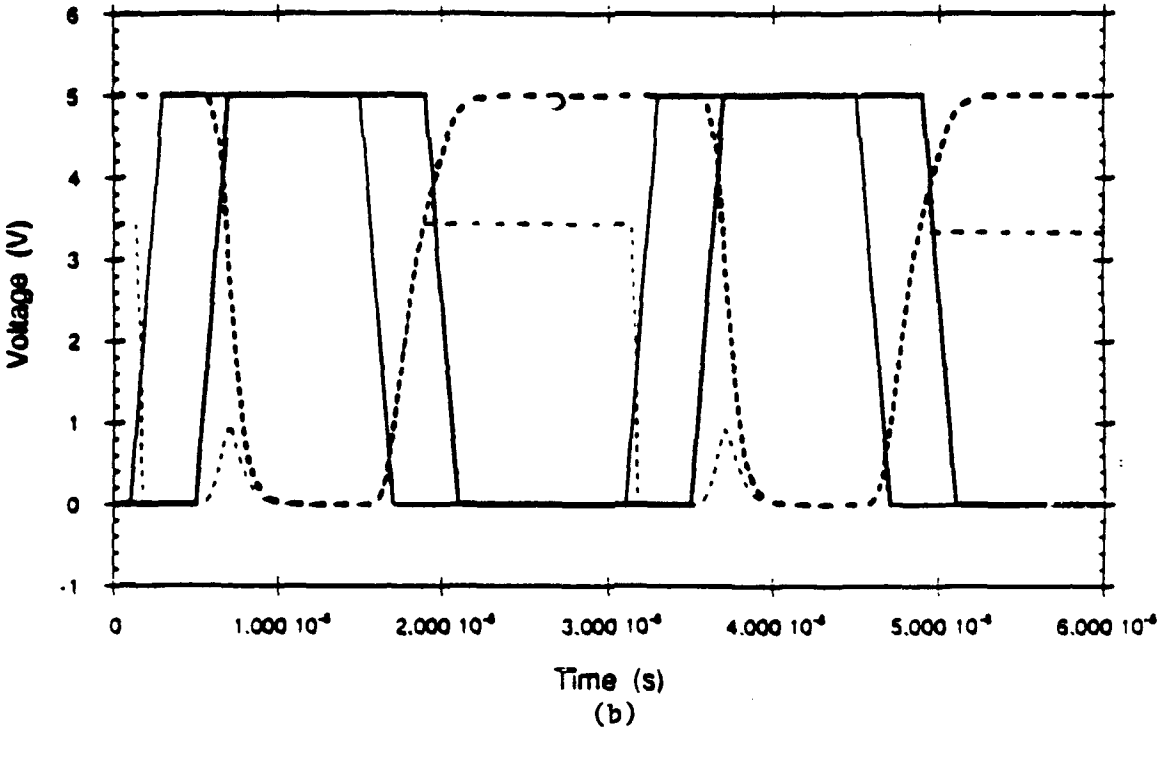


Fig. 8. Two-input CMOS NAND gate.



(a)



(b)

Fig. 9. Voltage waveforms of the two-input NAND gate with (a) positive and (b) negative input signal skew.

Thick solid line : Upper input voltage (V_{in1}).

Thin sold line : Lower input voltage (V_{in2}).

Thick dashed line : Output voltage.

Thin dashed line : Voltage across C_p.

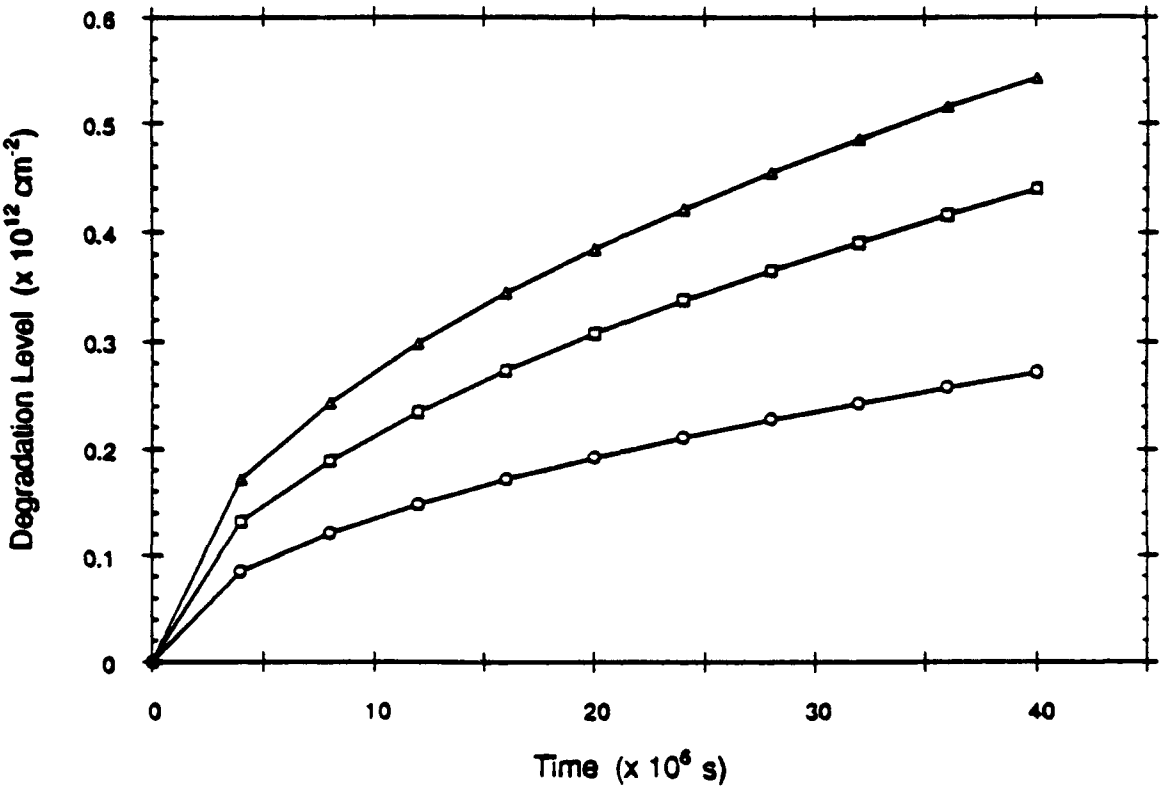


Fig. 10. Simulated degradation versus operation time of the upper nMOS transistor (M1) of the NAND gate, with three different input skew conditions.

○ : Input skew = + 5 ns

□ : Input skew = 0 ns

Δ : Input skew = -5 ns

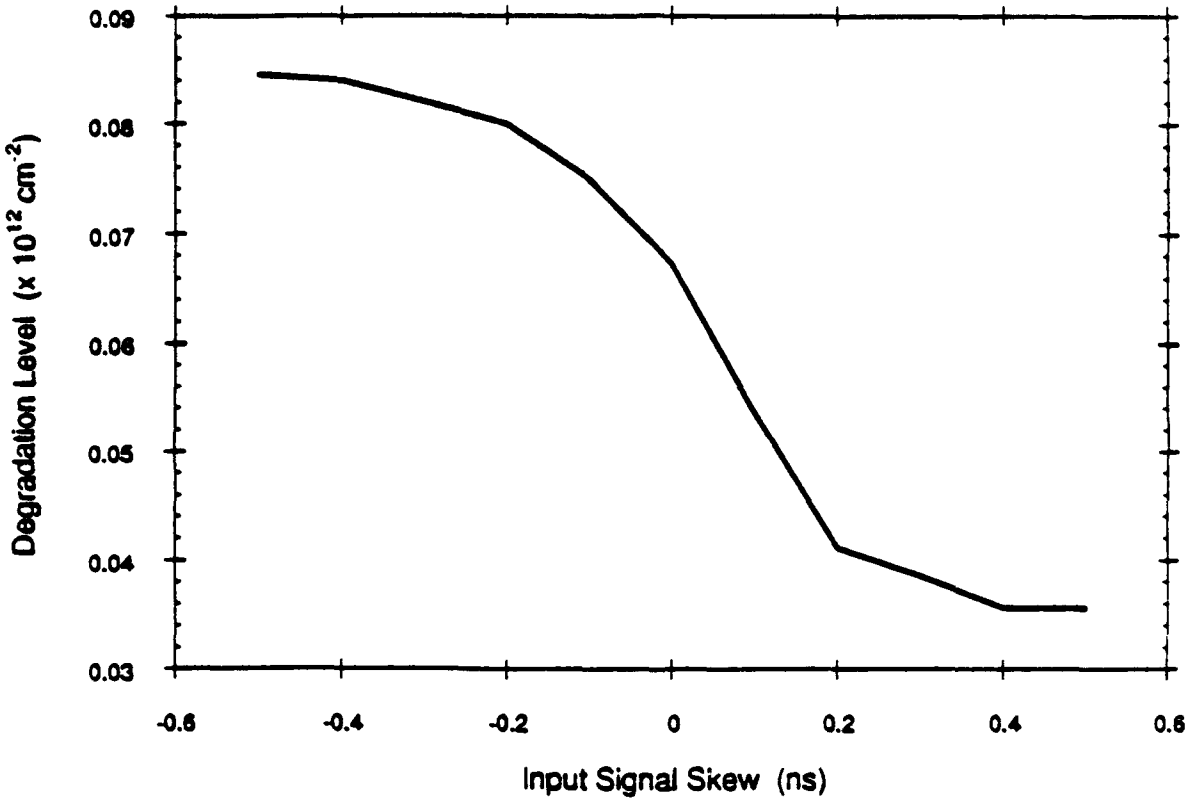


Fig. 11. Simulated degradation of M1 during $1x10^6$ sec of operation time, as a function of the input signal skew.

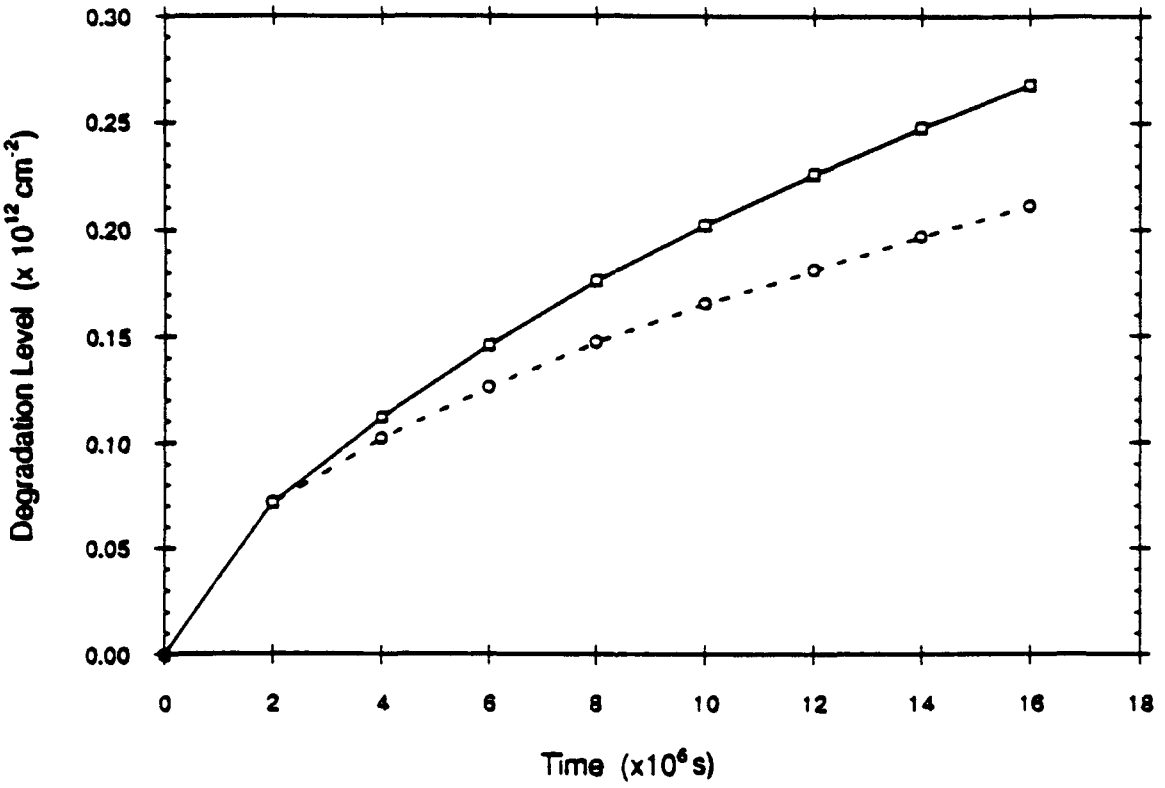


Fig. 12. Simulated degradation of M1 versus operation time where the upper input of the NAND gate is driven by the output of the inverter chain (solid line), and the degradation estimated by the one-cycle simulation approach (dashed line).

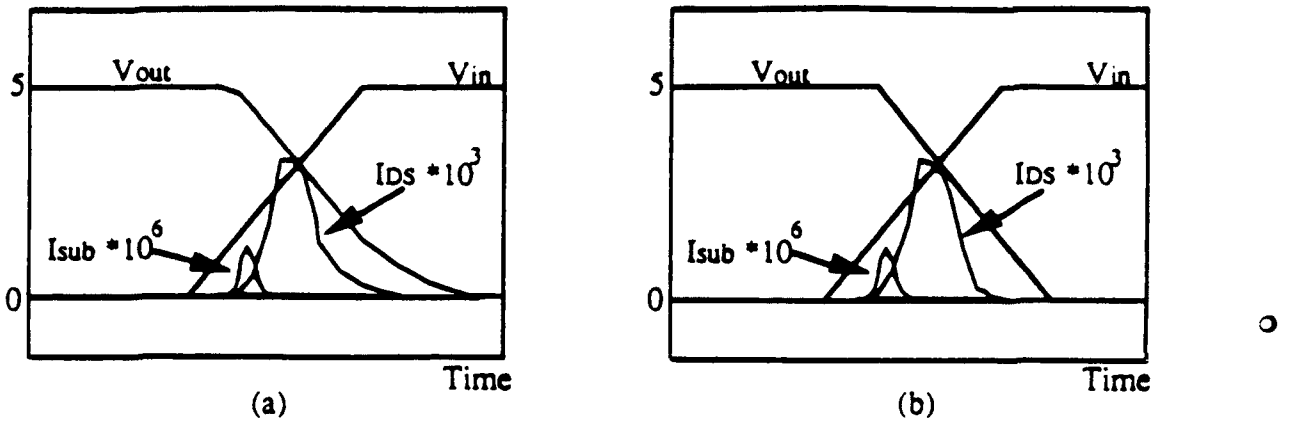


Fig. 13. (a) The waveforms of V_{in}, V_{out}, I_{DS}, I_{SUB} of the nMOS transistor of a CMOS inverter obtained using SPICE.

(b) The waveforms after replacing V_{out} with a ramp. The ramp is obtained by connecting the two points (t1, V_{out}(t1)=4) and (t2, V_{out}(t2)=1).

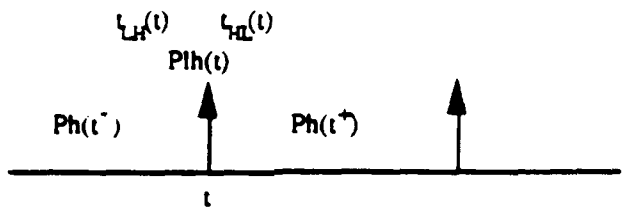


Fig. 15

Fig. 14. A typical input waveform for probabilistic timing simulation.

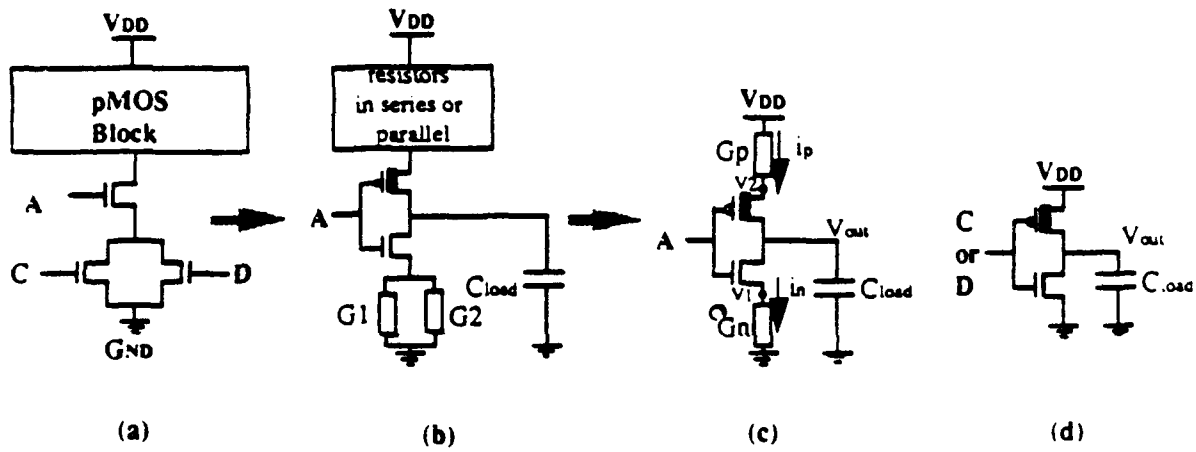


Fig. 15. (a) The conducting path of a CMOS circuit.

(b) Equivalent circuit.

(c) Macromodel for estimating i_n and i_p.

(d) Macromodel for estimating delay and output slew rate.

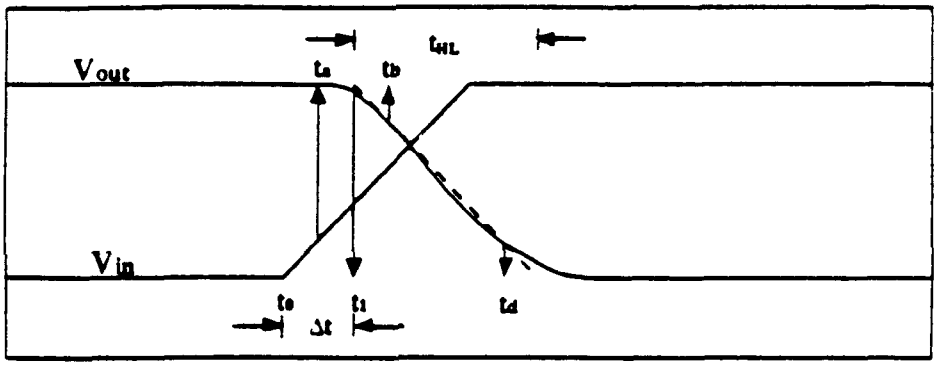


Fig. 16. A typical high-to-low transition.

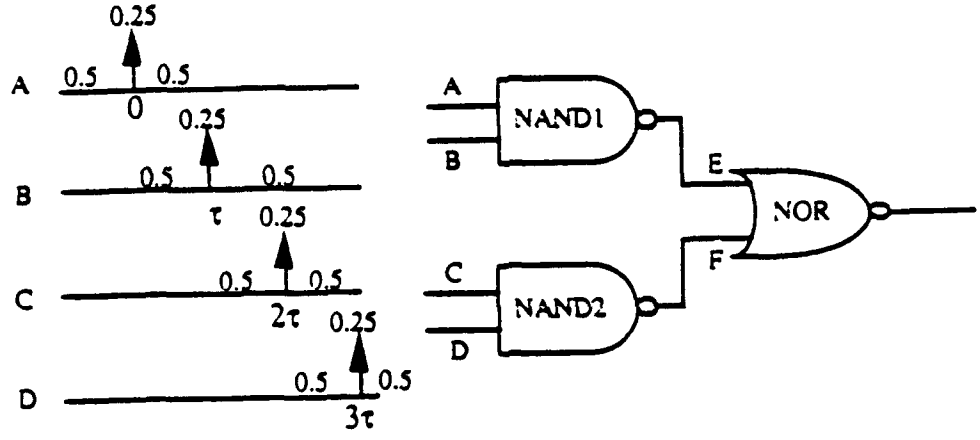


Fig. 17. A test CMOS combinational circuit and the input statistical descriptions. τ_{HL} and τ_{LH} are both 0.2 ns for each input event. Simulation period T = 20 ns.

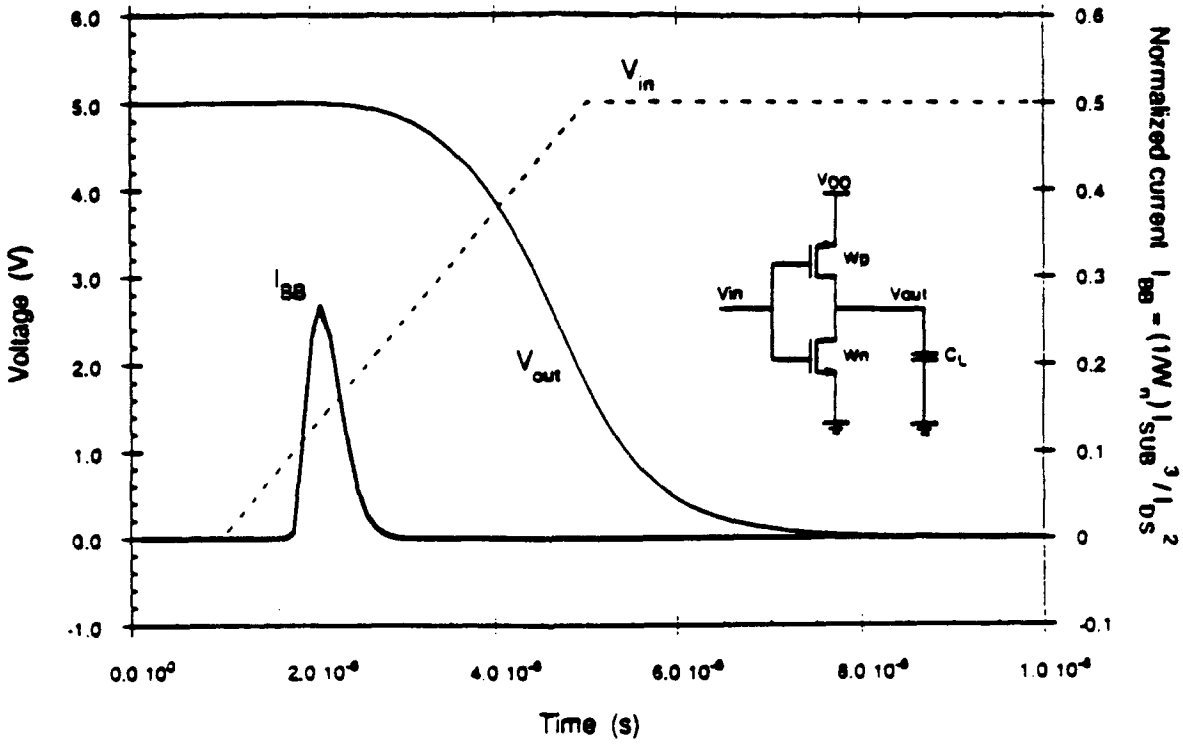


Fig. 18. Typical input/output voltage waveforms (thin lines) and the nMOS transistor bond-breaking current (thick solid line) for a CMOS inverter circuit (inset).

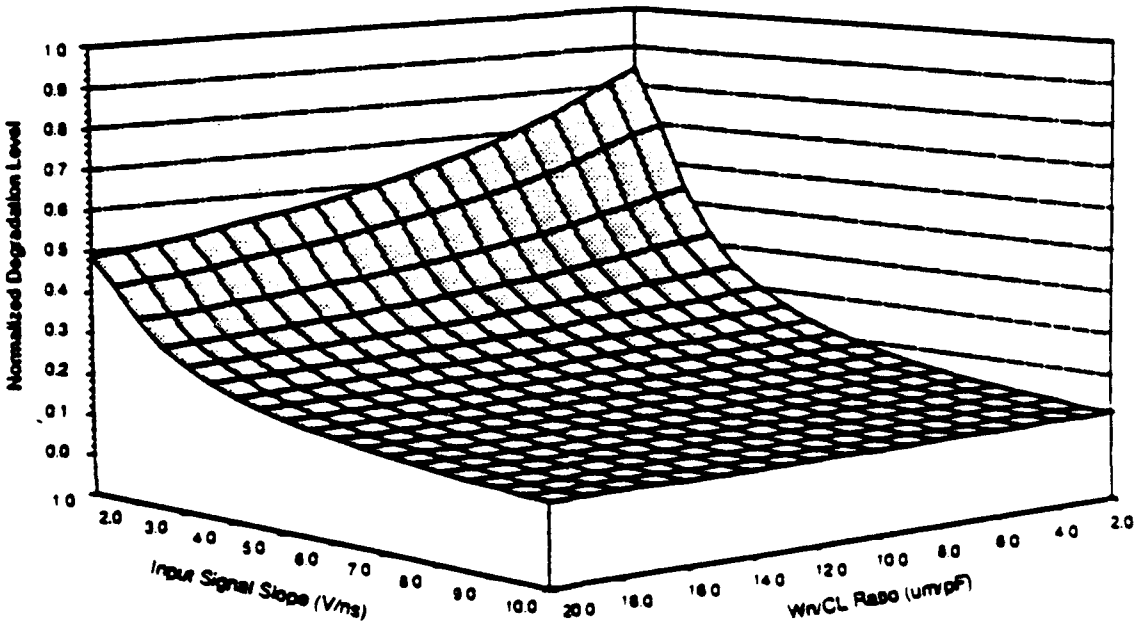


Fig. 19. Degradation of the nMOS transistor in the CMOS inverter circuit as a function of input signal slope a and the (W_n/C_L) ratio.

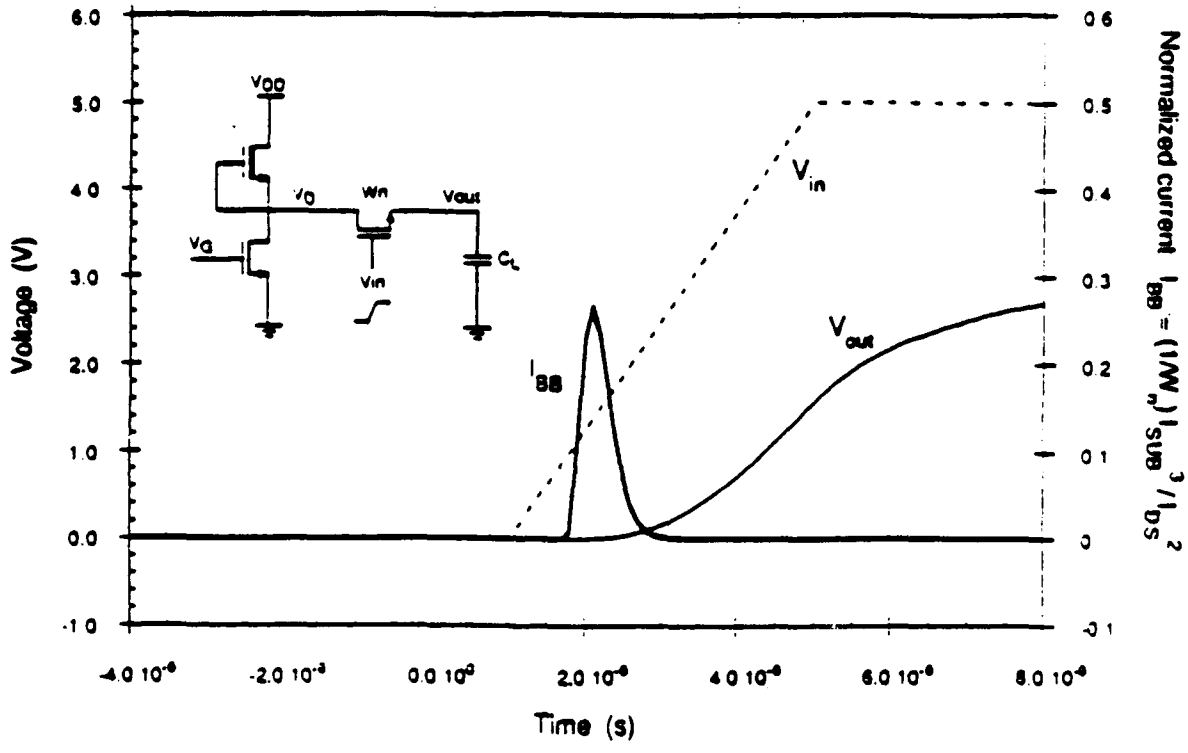


Fig. 20. Typical input/output voltage waveforms (thin lines) and the nMOS transistor bond-breaking current (thick solid line) for an nMOS pass-gate circuit (inset).

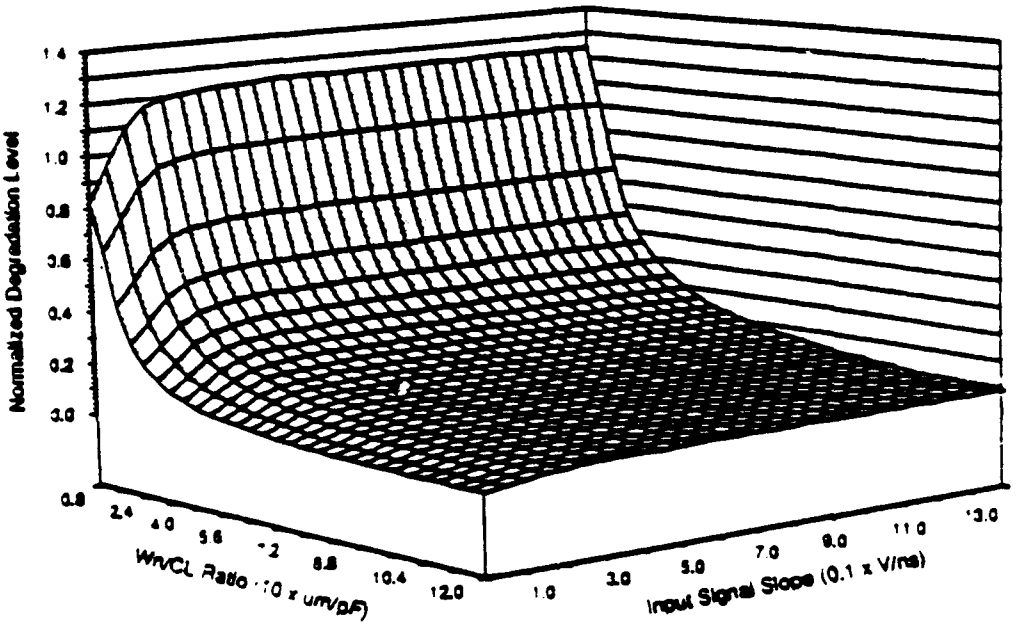


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Fig. 21. Degradation of the nMOS pass-gate transistor as a function of input signal slope a and the (W_n/C_L) ratio.

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